Ph.D. DISSERTATION

A SILICON SURFACE ION-TRAP CHIP WITH DIELECTRIC SIDEWALLS SHIELDED BY METAL FILMS

절연층 측벽을 금속 박막으로 보호한 실리콘 평면 이온트랩 칩

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Abstract

An ion trap is a device to confine charged particles by utilizing electromagnetic fields. Since the trapped ions have a feasibility of the individual state manipulation, a long coherence time, and an ideal isolation from the surroundings, the ion-trap technology becomes one of the leading candidates for the physical implementation of quantum information processing. In order to build a large-scale integrated ion-trap system for realizing complex quantum algorithms, microfabrication technologies have been applied to construct ion traps. The use of micro-electro-mechanical system (MEMS) ion-trap chip allows a scalable architecture of ion-trap arrays and integration of functional components to the trap chip, but a few side effects also arise. One of the most particular problems is stray fields generated by the charges accumulated on the sidewalls of thick dielectric pillars or the native oxide grown on metal surfaces, since the stray fields lead to ion micromotions which can cause heating and escape of the trapped ions. This dissertation presents a silicon surface ion-trap chip with dielectric sidewalls shielded by metal films. The oxide pillars supporting the top electrodes are fabricated to have overhang structures, and the upper and lower part of the pillars are coated by separate aluminum layers which are electrically isolated from each other. In order to evaluate the effects of the native

metal oxide on the electrode surface to the charging phenomenon, a trap chip with an additional gold layer on the aluminum electrodes is also fabricated. An ultra-high vacuum (UHV) chamber, electrical connections, and an optical setup are prepared to trap $^{174}Yb^{+}$ ions, and the ions are successfully trapped by using the experimental setup including the fabricated ion-trap chip. To evaluate the effectiveness of the proposed electrode structures, charging is intentionally induced on the chip surface by injecting a 355-nm pulse laser with 40-μW power perpendicularly to the chip surface. The intensity of the stray field is estimated by measuring the displacement of ion position after charging is induced. When the Al-based chips with exposed and Al-coated dielectric sidewalls are used, the standard deviation of the intensities of stray fields are 3.53, and 5.63 V/m, respectively. However, the standard deviation of the intensity of stray fields in the case of using Au-coated chip is 1.56 V/m, and any stray field is measured when the laser was injected on the surface or sidewalls of the gold-coated electrodes. These experimental results indicate that the gold coating on the surface of the aluminum electrodes and the sidewalls of dielectric pillars is effective for eliminating the generation of stray fields induced by static charges.

Keywords: Ion trap, Microfabrication, Quantum information processing, Dielectric charging, Stray field

Student Number: 2011-30979

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Chapter 1

INTRODUCTION

1.1 Quantum Information Processing and Qubit

Quantum information processing (QIP) is a novel information processing method based on quantum mechanics and uses two quantum states in a quantum system as a basic unit of information, instead of two voltage levels in conventional information processing based on electronics [1-3]. This basic unit is called “qubit”, an abbreviation for quantum bit (Fig. 1-1). The information stored in a single qubit exists in a superposition of two quantum states which indicates an arbitrary linear combination of two orthonormal basis $|\psi\rangle = a_0|0\rangle + a_1|1\rangle$, where a_0 and a_1 are complex probability amplitudes which allow $|a_0|^2 + |a_1|^2 = 1$. In addition, if we

consider a multi-qubit system, the qubits can be “entangled”, which means that the state of a qubit can be determined by the measurement result of the other qubit. For example, in the case of the two-qubit state given by $|\psi\rangle = \frac{1}{\sqrt{2}}|00\rangle + \frac{1}{\sqrt{2}}|11\rangle$, when the state of one qubit is determined, the state of the other qubit also collapses to the same state. Based on these phenomena in the quantum regime, QIP is expected to achieve noticeable increases in the speed in information processing problems. Therefore, many QIP applications such as quantum communication [4-6], quantum computer [7-9], and quantum simulator [10-12] have been proposed and are being actively researched.

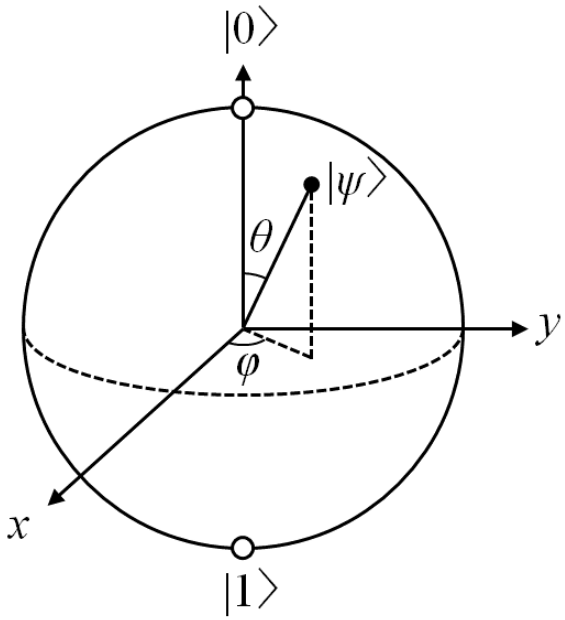


Figure 1-1. A Bloch-sphere representation of a qubit.

1.2 Ion Trap as a Qubit Platform

An ion trap is a device which can trap charged particles in space by using electric or electromagnetic fields. Trapping a charged particle with static potential alone is impossible because the static potential (φ) obeys one of Maxwell's equations $\nabla^2\varphi = 0$ [13]. Wolfgang Paul used an oscillating electric field together with the static electric field [14], and Hans Georg Dehmelt added a magnetic field to the static electric field to trap a positive ion [15]. The ion traps built by Paul and Dehmelt are called "Paul trap" and "Penning trap" respectively (Fig. 1-2). The ion traps were firstly developed for precise measurement systems used in fundamental physics applications such as optical clock and mass spectroscopy [16-18]. However, since a quantum algorithm utilizing ion qubits was proposed [19], they have also been actively explored as a physical platform to implement quantum information processing, attributed to the desirable characteristics of trapped ions as qubits such as long coherence times, ideal isolation in an ultra-high vacuum (UHV) environment, and feasibility of individual qubit manipulation [20-22], as well as satisfaction of DiVincenzo criteria [23]. In recent years, the ion trap system is considered as the most advanced qubit technology, owing to the development of extremely-high-fidelity qubit operations [24], entanglement among more than ten qubits [25], and

programmable quantum computer module (Fig. 1-3) [26].

Figure 1-2. The first Paul trap built by Wolfgang Paul [14].

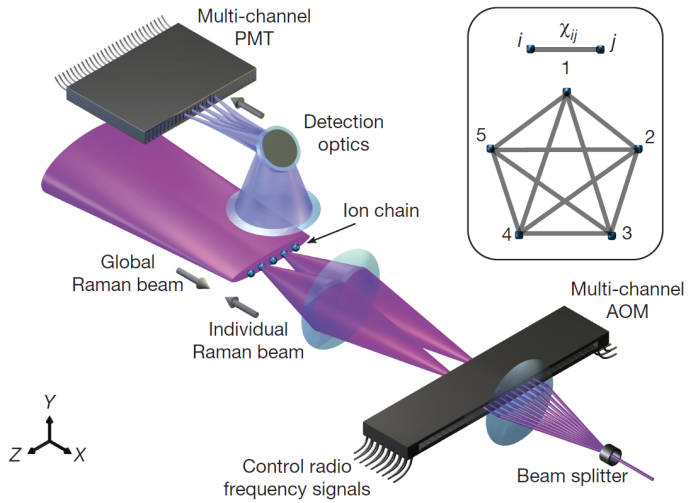


Figure 1-3. Computation architecture proposed in Reference [26].

1.3 Development of Surface Ion Trap

To implement more complicated quantum operations, a concept of integrating multiple ion trap arrays in a single ion trap chip was proposed [27]. The ion-trap chip integrated with multiple ion-trap arrays consists of operation regions in which the quantum operations are held, memory regions that stores ions conserving qubit states, and regions for loading ions. Scalable microfabrication technologies were applied for the implementation of these large-scale integrated ion traps, and the first microfabricated ion trap chip implemented the 4-rod ion trap configuration using a semiconductor fabrication process (Fig. 1-4) [28, 29]. In this method, however, the asymmetric configuration of the four electrodes results in a low radial confinement, which in turn leads to a fast ion loss. To overcome the limitation of implementing a 3-D structure using essentially 2-D fabrication techniques, a breakthrough in the 2-D planar ion trap where all electrodes are laid in the same plane was proposed [30-32]. This is more suitable for the microelectromechanical system (MEMS) fabrication technology. These 2-D ion traps are called the “surface ion traps” or “surface traps” (Fig. 1-5). The surface traps have advantages in the scalability, and are now more widely used by many research groups.

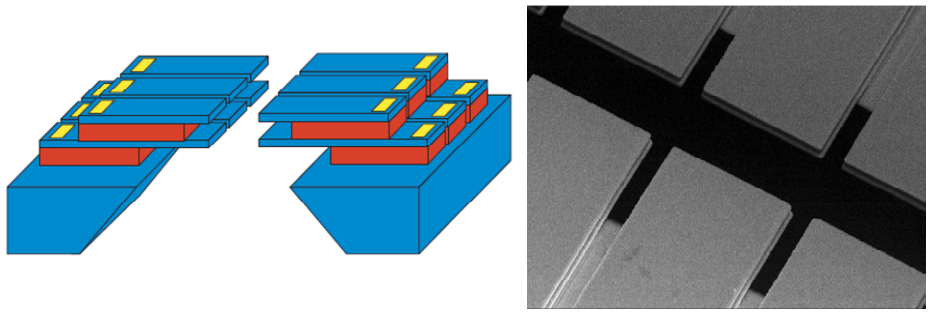


Figure 1-4. The first ion-trap chip fabricated by using a semiconductor process [28].

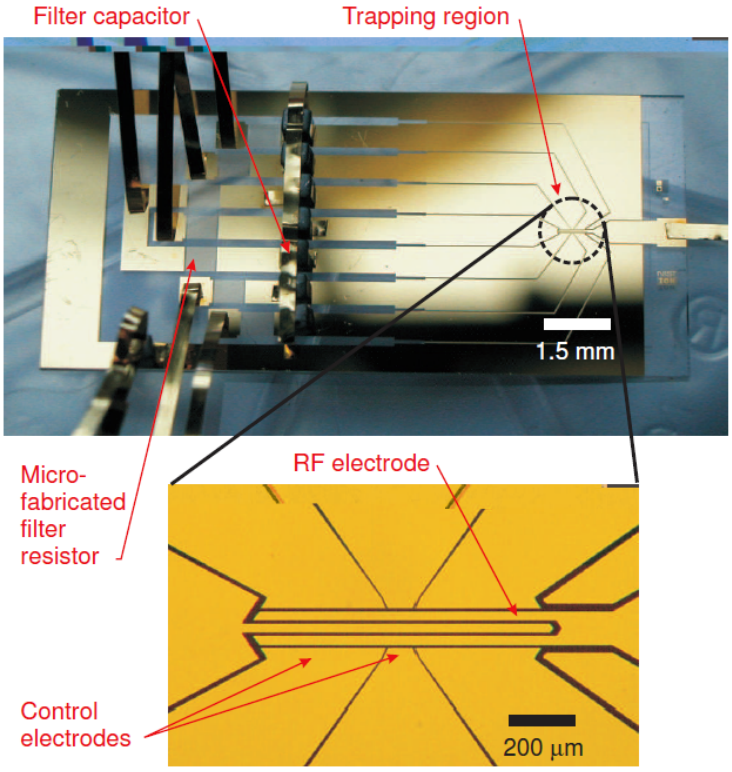


Figure 1-5. The first ion-trap chip in a planar electrode structure [30].

The first surface trap is fabricated by patterning a single Au electrode layer on a non-conductive substrate such as quartz or sapphire [30, 33], but these simple fabrication methods cannot be used to fabricate complex ion trap structures. To overcome this limitation, a surface trap chip with multi metal layers which are fabricated on a silicon substrate has been being researched [34, 35].

Figure 1-6 shows a simplified schematic of a surface ion trap. The black arrows show the direction of the electric field during the positive phase of the radio-frequency (RF) voltage, and the green dot represents a trapped ion. An RF voltage is applied to the pair of RF electrodes while all the other electrodes are kept at RF ground, and the ponderomotive potential generated by the RF voltage confines the ions in the radial direction [32]. The direct current (DC) voltages applied to the multiple DC electrodes designed outside the RF electrodes confine the ions in the longitudinal direction. The inner rails between the RF electrodes are designed to help tilting the principal axes of the total potential in the transverse plane.

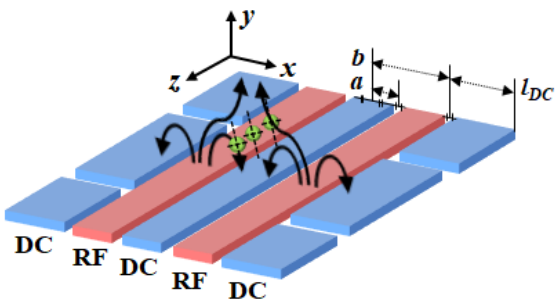


Figure 1-6. Simplified schematic of a surface ion-trap chip.

1.4 State-of-the-Art of Surface Ion Trap

1.4.1 Advanced Technologies

a. Junction Traps

In order to adapt more complex quantum algorithms, a multi-zone ion trap composed by a number of ion trap arrays is proposed [27]. In this multi-zone ion trap, the trapping zones are connected by “X” or “Y” junctions, and the information stored in ions can be transferred from one zone to another through the junctions. Ion transports via junctions however require not only applying DC control voltages, but more complex techniques, because pseudopotential barriers created by RF voltages exist near the center of the junctions. Therefore, the geometries near the junctions should be optimized by an iterative algorithm to minimize the magnitude of the pseudopotential barriers [36, 37]. Recently, selective ion transports through junction nodes have been demonstrated either on the conventional traps [38, 39] and the surface traps (Figs. 1-7, 8) [40-42].

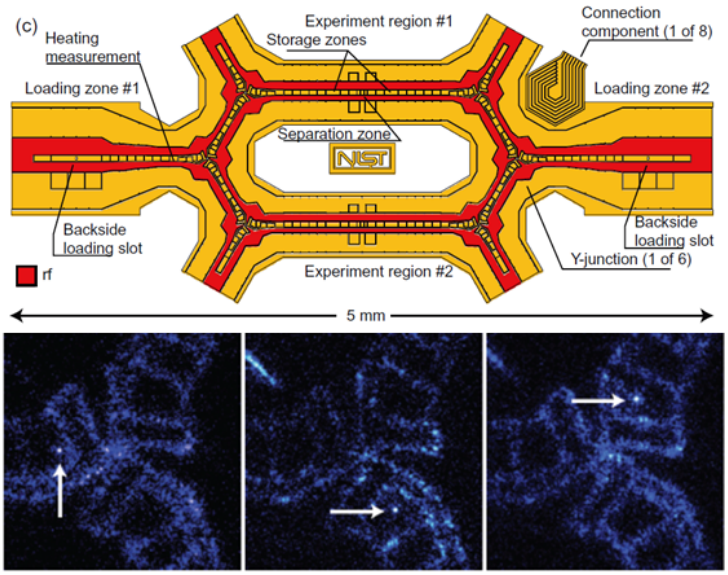


Figure 1-7. Surface ion-trap chip with a Y-junction node [40].

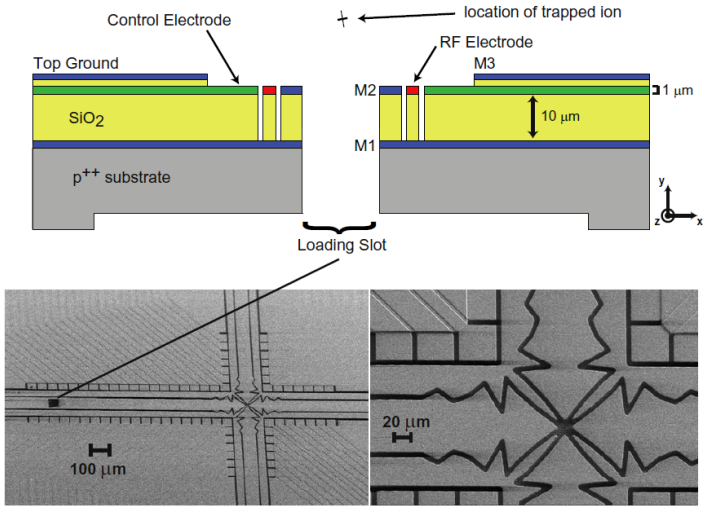


Figure 1-8. Surface ion-trap chip with a X-junction node [41].

b. Near-Field Microwave Circuit

To realize a large-scale integrated qubit system based on the ion-trap technology, manipulation of the qubit states as well as the trap geometries need to be scaled-up. However, a laser based system or a long-wavelength radiation of microwave which are widely used in current ion-trap researches are not compatible with a large-scale architecture. To solve this problem, Ospelkaus *et al*. proposed using magnetic field gradients near microwave strips integrated on a surface ion trap chip to induce qubit operations (Fig. 1-9) [43]. Recently, a significantly high fidelity of the qubit gates has been reported by Harty *et al*. [24] using this method, then this near-field microwave technique is considered as a promising architecture for scalable qubit manipulations.

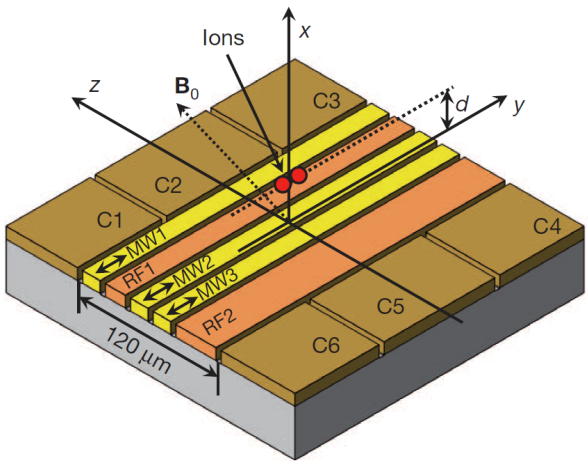


Figure 1-9. Schematic of a ion-trap chip integrated with a microwave circuit [43].

c. Integration of Optical Components

Optical components used in the ion trap experiments are to be placed as near as possible to the ions, and precisely aligned with respect to the ion position. To fulfill both requirements, integration of optical components to the ion trap chip has been being intensively explored. To increase the photon collection efficiency, a surface ion trap chip with a metal mirror fabricated between the RF electrodes was developed (Fig. 1-10) [44]. Moreover, an ion trap chip even fabricated on a macroscopic mirror was reported [45]. In addition, an ion trap chip which integrates optical waveguides in its substrate was developed to address lasers to the trapped ions without misalignment (Fig. 1-11) [46].

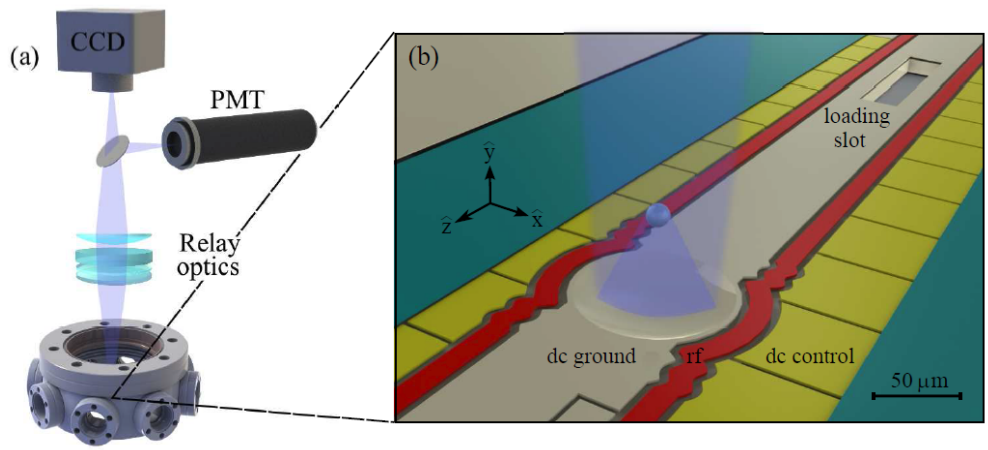


Figure 1-10. Surface ion-trap chip integrated with a metal mirror [44].

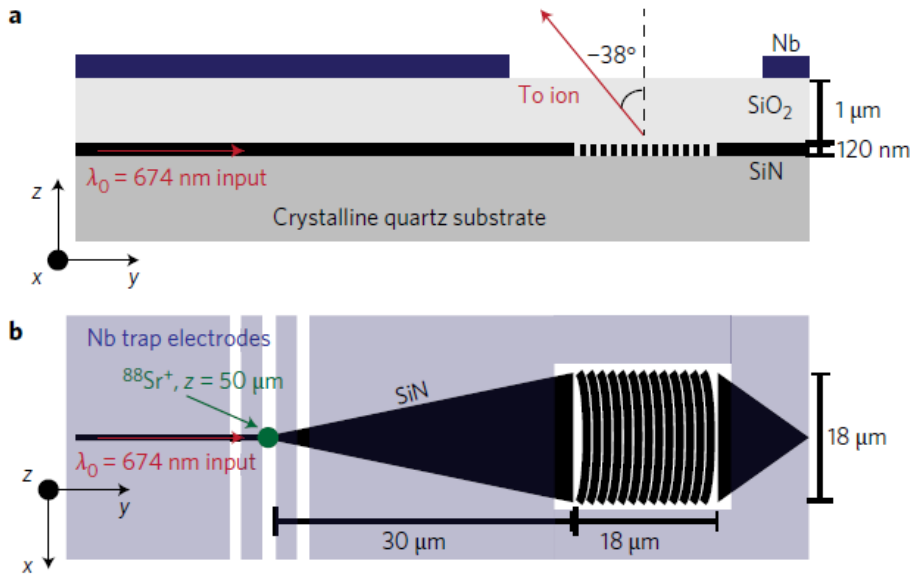


Figure 1-11. Surface ion-trap chip integrated with an optical waveguide [46].

d. Integration of Trench Capacitors

Most research groups using surface ion traps try to eliminate the RF pickup on the DC electrodes by connecting capacitor chips to each DC electrodes [33, 35]. This method is effectively used in these days, but the manual assembly of capacitor chips is not suitable for the construction of scalable systems. Thus, trench-type capacitors fabricated in the silicon substrate have been developed. For example, Guise *et al*. [47] integrated trench capacitors in an ion trap chip (Fig. 1-12), and trench capacitors fabricated on an interposer chip was also reported [48].

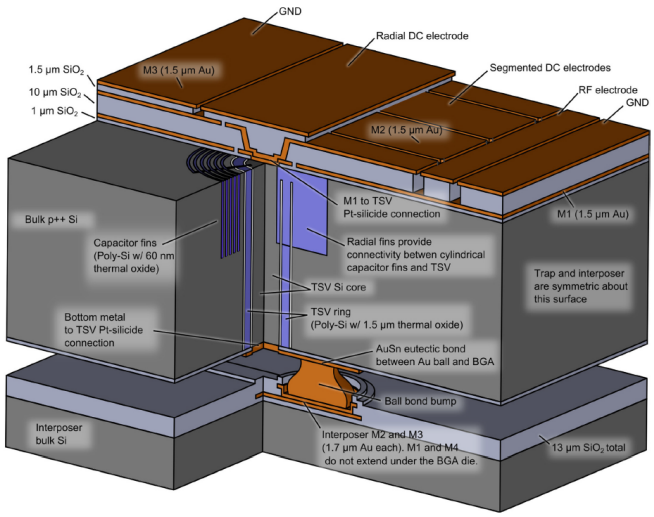


Figure 1-12. Schematic of a ion-trap chip integrated with trench capacitors [47].

1.4.2 Current Challenges

Although application of MEMS fabrication technologies allows a scalable architecture of ion-trap arrays and integration of functional components to the trap chip, some unwanted side effect also arise attributed to the miniaturization of the ion traps. Anomalous heating of trapped ions and charging of dielectric materials are representative problems.

a. Anomalous heating

The heating of trapped ions by electric field noise is called “anomalous”, because the sources of the heating are still not clearly understood. This heating is particularly important problem because it can limit the fidelity of multi-qubit

entangling gate operations utilizing motional modes. Furthermore, since the noise spectral density is approximately proportional to d^{-4} where d is the ion-electrode distance [49], the heating can be more serious problem especially in the case of the microfabricated ion trap chip which traps the ions close to the electrodes. Therefore, the heating of the ions trapped on the microfabricated traps has been widely studied [50, 51]. Among the various efforts to reduce the anomalous heating, in-situ cleaning which can remove contaminants on the chip surface is considered as the most effective method (Fig. 1-13) [52, 53]. In addition, cooling the ions to the cryogenic temperature which seems to suppress the thermally activated noises is also an efficient method (Fig. 1-14) [54, 55].

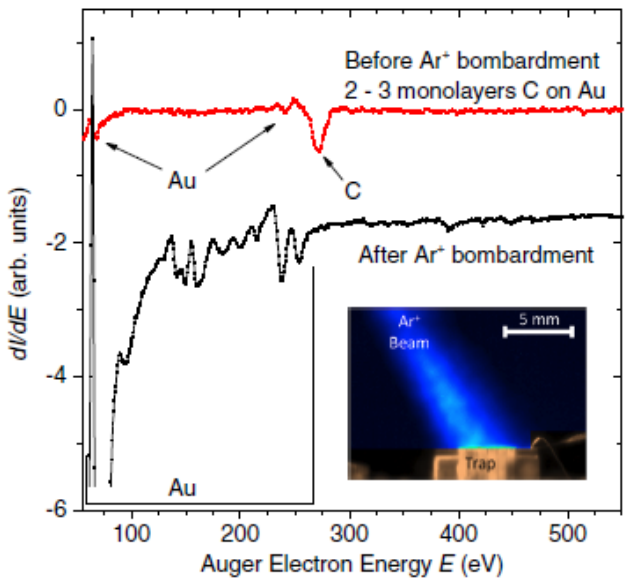


Figure 1-13. *In-situ* cleaning of electrode surface using Ar beam [52].

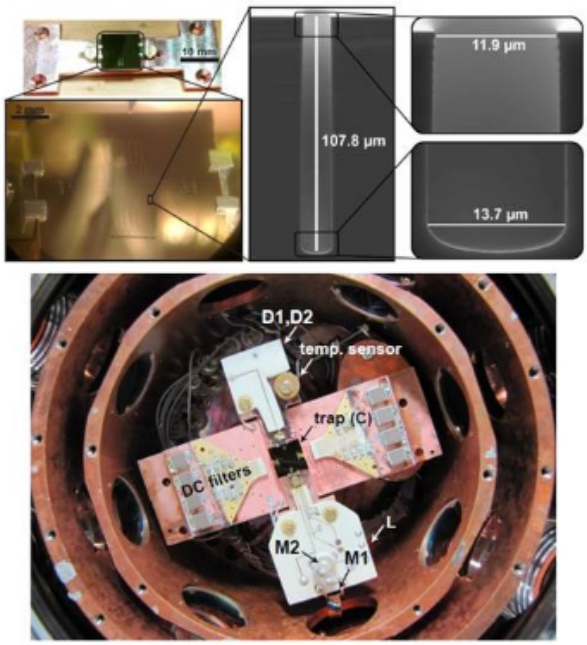


Figure 1-14. Ion-trap system for cryogenic experiments [55].

b. Dielectric charging

Illuminating laser lights on a trap surface can induce charges by photoelectric effects. The charging mechanisms are different for the charging of bulk dielectrics and thin native oxide grown on the metal surface [55]. When laser is illuminated on the bulk dielectric structure such as the sidewalls of dielectric pillars, the trapped ions is repulsed by the positive charges accumulated on the dielectric surfaces. The origin of this phenomenon is not understood well because the work function of the dielectric material is generally greater than the energy delivered from the ultra-violet (UV) lasers. However, this kind of charging has been steadily reported in the ion

trap community [45, 55]. Positive charges built up on bulk dielectrics do not easily dissipate, and lead to the excessive micromotion. The ion trap chip fabricated on a silicon substrate generally has exposed dielectric surfaces on the sidewall of the thick dielectric pillars supporting electrodes. To reduce the area of exposed dielectric surfaces, Stick *et al*. proposed an ion-trap chip with an electrode overhang structure (Fig. 1-15) [56], and Niedermayr *et al*. proposed an ion-trap chip with a deep trench between electrodes [57]. However, these structures cannot entirely eliminate exposing dielectric surfaces from trapped ions.

The second charging phenomenon is occurred when the UV laser is injected to a metal surface with a thin native oxide film on it [58]. Photoelectric effects are induced on the metal surface, but the negative charges cannot be released to the free space due to the thin dielectric film on the metal surface. Thus, the attractive force from the negative charges confined in the dielectric films is applied to the trapped ion with a positive charge. This kind of charging on the microfabricated ion-trap chips is studied by Wang *et al.* [59], though the report did not consider the effects from the dielectric surfaces exposed between the electrodes. Agreeing with the results in [59], gold is the most preferred material for the ion-trap electrodes because any native oxide is grown on the gold surfaces. Unfortunately, gold is not available with most conventional semiconductor processes.

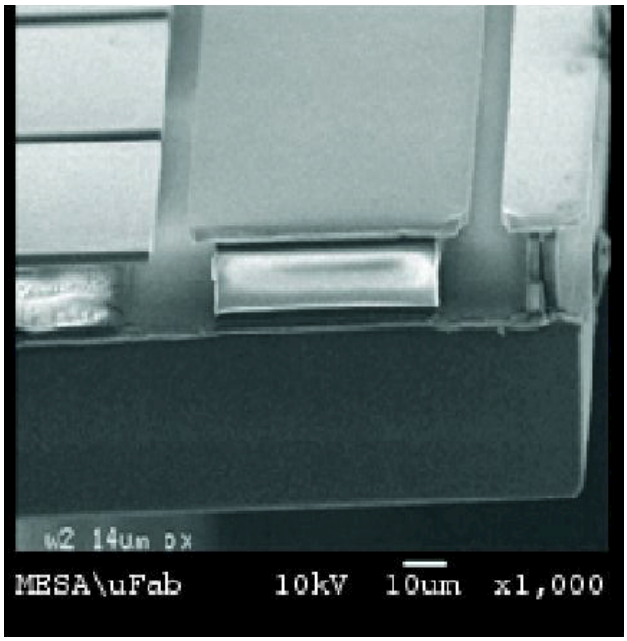


Figure 1-15. Surface ion-trap chip with electrode overhang structures [56].

1.5 Document Overview

In this dissertation, a silicon surface ion-trap chip with dielectric sidewalls shielded by metal films is proposed. In order to prevent the dielectric sidewalls to be exposed to the trapped ions, metal film is coated on the surface of the dielectric sidewalls. The metal films coated on the upper and the lower part of the oxide pillars are electrically isolated by overhang structures of the oxide pillars. To fabricated the proposed structure, a sacrificial process has been designed and developed. The fabrication process mainly uses aluminum for the conducting material.

However, another version of chip which has an additional gold layer on the electrode surfaces has also been fabricated to inspect the effect of the native oxidation of the aluminum surfaces. The fabricated chip has been successfully implemented to trap $^{174}Yb^{+}$ ions. Also, the effectiveness of the shielding the dielectric surfaces has been investigated by illuminating ultra-violet (UV) laser on the surface of the fabricated chips and measuring the distance that the position of the trapped ion is axially shifted. (The experimental results will be updated here.)

Following this introduction, chapter 2 provides a design of the surface ion-trap chip. In this chapter, the proposed electrode structure of surface ion-trap chip is explained more specifically. After that, the details of layout design including a brief explanation of the backgrounds, a simulation method, and a design philosophy are presented. Finally, the mask layout of the proposed chip is designed.

Chapter 3 provides overview of the fabrication processes. The information of used materials and semiconductor equipment is presented first. Then, the fabrication process of the surface ion-trap chip with aluminum electrodes, and a gold coating process which can be added to the main process are presented. Finally, the fabrication results are presented.

The Experimental setup and results are provided in chapter 4. The preparation

of the experimental setup to trap $^{174}Yb^{+}$ ions are discussed. Also, the experimental results of the dielectric charging experiments, to investigate the effectiveness of the proposed ion-trap structure, are presented.

Finally, in chapter 5 the obtained results are summarized and concluded. Future works towards the realization of surface ion-trap chip robust to the dielectric charging effects is presented, as well as some suggestion for enhancing the performance.

Chapter 2

DESIGN

2.1 Structural Design

2.1.1 General Considerations for Structural Design

Typical silicon-based ion-trap chips have basically two metal layers [60]. The first one right on the silicon substrate is called “ground plane” and prevents loss of the RF signal through the substrate. The second one atop the entire structure provides the RF electrodes and DC electrodes. Between these metal layers, a thick dielectric layer is deposited to prevent the electrical breakdown. The dielectric layer is patterned to have pillar-like shapes supporting the top electrodes, not to reveal its top surface directly to the trapped ions. Generally, the thicker dielectric layer is

preferred, since it allows the application of a higher RF voltage. The higher RF voltage enables trapping ions further from the chip surface. The higher ion height can decrease the electrical field noise from the chip surface which easily induce the anomalous heating, and the laser scattering by the chip surface. Currently, the thickness of the dielectric layer is over 10 μm.

In the surface ion-trap technologies, all the materials including various deposited films should be able to withstand a long-term bake-out at the temperature near 200 °C, and the amount of outgassing from all materials should be compatible with UHV environments. Thus, the surface ion trap chips presented in this dissertation composed of single crystalline silicon, silicon dioxide, aluminum, and gold, whose compatibility for the bake-out and the UHV environment has been demonstrated by various previous experiments.

A through hole which penetrates the silicon substrate is required for loading neutral atoms from the back side of the chip. The atom loading from the back side is useful because it does not occur the deposition of the neutral atoms on the gaps between the electrodes which occasionally leads to the electrical shorts between the neighboring electrodes. This via hole also allows the laser beam path penetrating the chip substrate in the perpendicular direction [48].

The scattering of laser light by the bonding wires should be minimized.

Generally, the electrodes of the ion-trap chip are connected to the pins of chip carrier or directly to the printed circuit board (PCB) by the bonding wires. These wires must not be placed near the beam path and interfere the propagation of the laser beam, and the bonding pads should be designed considering the beam paths in the layout design step. Alternatively, a low-loop wire bonding method (Fig. 2-1) [62] or wiring using a through silicon via (TSV) method can also be used to prevent the beam scattering by the wires. In addition, a Gaussian beam whose radius increases according to the distance from the beam waist can be clipped by the chip body near the chip edge. Therefore, the chip size need be minimized as possible. This factor will be further discussed in the layout design step.

Lastly, as mentioned in 1.4.2, the exposed area of the dielectric surfaces need be minimized. For this purpose, electrode overhang structures in [56] can be adopted. The overhang structures also allow the deposition of additional metal film such as gold on the electrode surfaces to prevent the native oxidation of metal surface.

These requirements are shown in our ion-trap chip in the previous generation (Fig. 2-2). Note that the layout design of this chip benchmarked that of Thunderbird Trap of Sandia National Lab. [56]. The detailed information for the fabrication process and the characteristics of the chip is not provided in this dissertation but presented in [61]. However, the evaluation of simulation tool and the charging

experiments using the chip is included in the remaining of this dissertation.

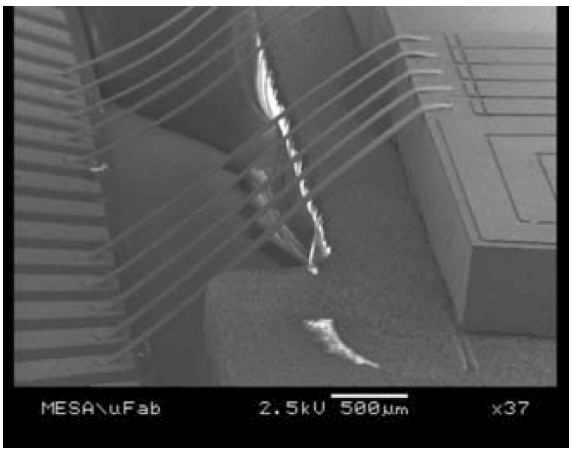


Figure 2-1. Low-loop wire bonding to avoid beam scattering by the wires [62].

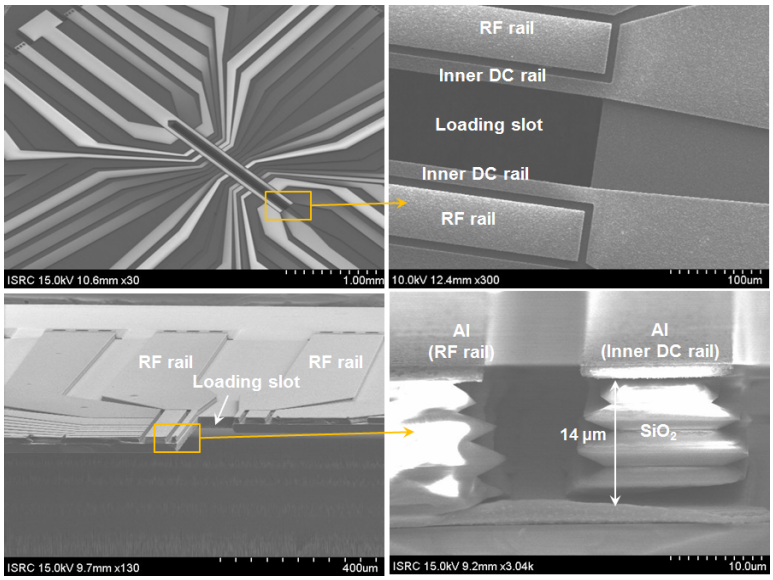


Figure 2-2. Our ion-trap chip of previous version [61].

2.1.2 Proposed Structure

A schematic of the proposed structure is shown in Figures 2-3, 4. There are three metal layers and three insulating layers in the final structure. The first insulating (I1) layer is deposited on the silicon substrate to insulate the first metal (M1) layer and the silicon substrate. The M1 layer provides inner DC electrodes and a ground plane. The arrangement of the inner DC rails on the M1 layer brings some difficulties in the fabrication process. Because the metal layer deposited on the sidewall of the dielectric pillars should be patterned to electrically isolate the inner DC rails and the ground plane. Nevertheless, the inner DC electrodes are laid on the M1 layer instead of the top metal (M3) layer to reduce the scattering of the laser beam right under the ion position. This is important because the fluorescence from the ion and the background scattering cannot be distinguished, so that the accuracy of the qubit operation can be decreased. The dielectric pillars consist of two insulating layers, I2 and I3, which are separately deposited and patterned. The sidewalls of the I2 and I3 layers are covered by the second metal (M2) layer and the M3 layer, respectively. The lateral gaps between the two dielectric layers realize the overhang structures which separate the M2 and M3 layers. The M3 layer also provides the RF and the outer electrodes. The proposed structure, of course, has a loading slot between the inner DC electrodes.

Since the RF breakdown voltages in UHV environment do not obey the Paschen's law, the dimensions of the gaps between the individual metal electrodes (including the ground plane) have no choice but to be determined by considering the RF dielectric strength which are heuristically estimated through our previous experiments [61]. It has been investigated that the 8-μm gap in 10^{-11}–Torr vacuum space can withstand the RF voltage with the amplitude over 240 V_{p-p}. This value provides the reference for designing the gaps between the conductors. Figure 2-4 shows the dimensions for the insulating gap among each electrodes. The lateral gap between the M3 layer on the sidewall of the I3 layer and the M2 layer on the sidewall of the I2 layer separated by the oxide overhang structure is determined to be 8 μm. The vertical gap between the M3 layer on the sidewall of the I3 layer and the M2 layer on the surface of the inner DC rails is also determined to be 8 μm. On the other hand, the vertical gap between the surface of the M3 layer and the top of the M2 layer on the dielectric sidewall is designed as 4 μm, since they are isolated by silicon dioxide whose dielectric constant is 3.9 times higher than vacuum space. The thickness of the I1 layer is 1 μm because no RF voltage is applied to the I1 layer.

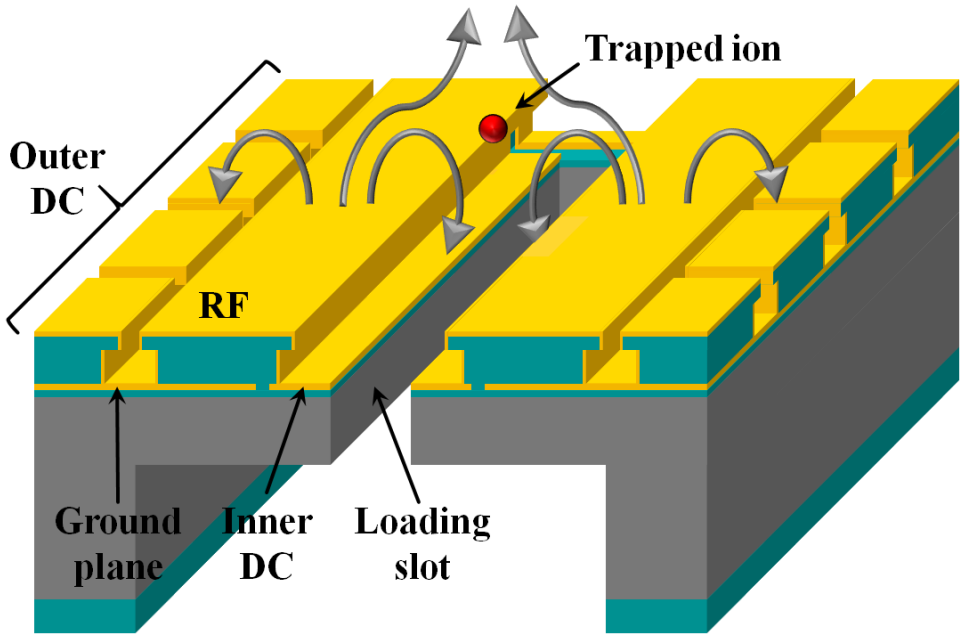


Figure 2-3. Schematic of the proposed surface ion-trap chip.

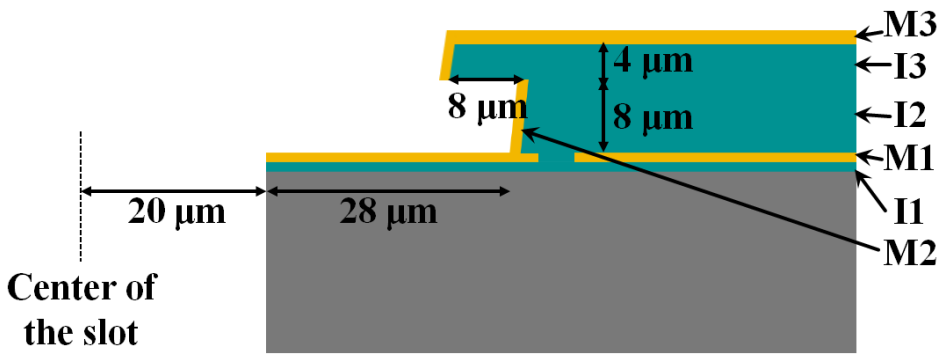


Figure 2-4. Schematic showing the cross-sectional dimensions.

2.2 Layout Design

2.2.1 Considered Parameters

A layout design of an ion-trap chip, especially near the trapping region, can determine various trap parameters which represent the performance of the trap chip. The physical meaning of some important parameters and the trade-off among them are described as follows.

a. Trap Depth

Trap depth is the difference in the total potential (sum of electric pseudopotential and DC potential) between the RF null and the saddle point, which is a stationary point but not a local extremum (Fig. 2-5). Deeper trap depths suppress the loss of ions induced by background gas collisions and increase ion lifetime. Surface ion traps have an inherently shallower trap depth that is barely above the mean kinetic energy of the evaporated neutral atoms [31]. Therefore, maximization of trap depth is frequently considered as a design goal for a surface ion trap.

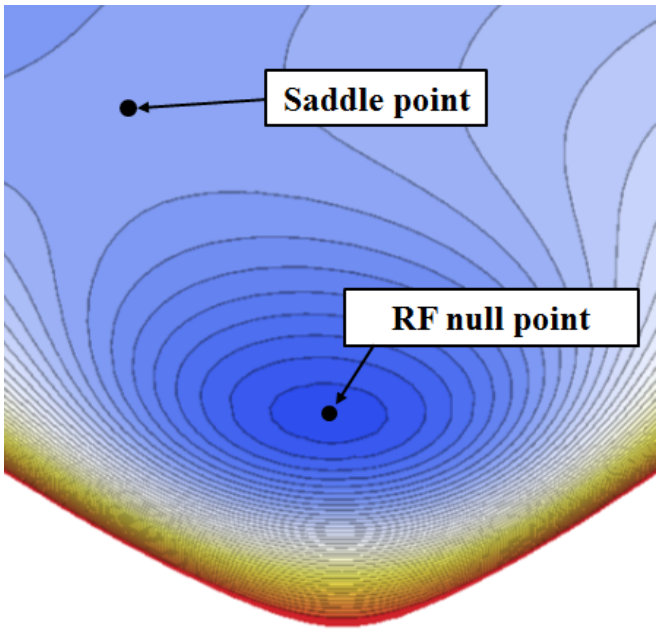


Figure 2-5. An example of the contour plot of the total potential.

b. q-Parameter

The classical radial motions of ions trapped in hyperbolic electrodes can be described by the standard Mathieu differential equation [64]:

$$\frac{d^2 i}{d\tau^2} + \left(a_i - 2q_i \cos 2\tau\right) i = 0, \quad i = x, y \tag{1}$$

where τ, a_x, a_y, q_x, and q_y are given below:

$$\tau = \frac{\Omega t}{2}, \quad a_x = -a_y = \frac{4eU}{mr_0^2\Omega^2}, \quad q_x = -q_y = \frac{2eV}{mr_0^2\Omega^2} \tag{2}$$

and Ω, *t, e, m, r_0, U,* and *V* indicate the RF voltage angular frequency, time, elementary charge, ion mass, ion–electrode distance, offset voltage, and RF voltage amplitude, respectively. In addition, the q-parameter is related to the secular frequencies and amplitudes of ion micromotion. The motion of the ion in the x-direction is described as follows [64]:

$$x = x_0 \cos\left(\beta_x \frac{\Omega}{2} t\right)\left[1 - \frac{q_x}{2}\cos(\Omega t)\right],\ \omega_{s,x} = \frac{\beta_x \Omega}{2}$$
$$\beta_x \approx \sqrt{a_x + \frac{{q_x}^2}{2}},\ q_x \approx 2\sqrt{2}\frac{\omega_{s,x}}{\Omega}\left(\text{when } a_x = 0\right) \quad (3)$$

where x_0 and $\omega_{s,x}$ indicate the oscillation amplitude of secular motion along the x-direction and the secular frequency along the x-direction, respectively (similar to the y-direction). Typically, the stable region usually used for hyperbolic electrode traps includes *a* and *q*, where $q < 0.7$ and $|a/q^2| < 0.5$ [16]. However, the stable region of *a* and *q* for a surface ion trap varies with the tilted angle of the principal axes, which is dependent on the geometries of the DC electrodes and the arrangement of the DC voltage. Because of the calculation complexity of the analytic derivation, an appropriate q-parameter value between 0.1 and 0.3 is generally considered as a starting point for design, and an optimal q-parameter can be determined as the experiment proceeds within stable ranges.

c. Secular Frequency

Secular frequency can be derived from the Mathieu parameters, as shown in Eq. (3), and can be expressed as follows:

$$\omega_{s,i} = \frac{e}{m}\frac{d^2\phi}{di^2}, \quad i = x, y, z \tag{4}$$

where ϕ is the total electric potential, which is the sum of the electric pseudopotential and static potentials. A higher secular frequency is preferred because it allows for tighter confinement, faster ion transportation [65], better cooling and less sensitivity to external noise [66]. Higher secular frequencies are also preferable for multi-qubit entangling gate operations utilizing motional modes [19]. Radial secular frequencies are strongly influenced by the electrode dimensions and are considered in the design of RF electrodes. The axial secular frequency is determined by adjusting both the DC voltages and the electrode geometry. When the peak voltage on the DC electrodes are limited by digital-to-analog converters, the maximum electric potential generated by a given electrode geometry can also be limited. Thus, occasionally, the designed electrode dimensions do not provide sufficiently high axial secular frequencies. Therefore, the effects of the DC voltage at the RF null point must be investigated after designing the RF electrodes.

d. Ion Height

The ion height is the vertical distance between the RF null point and the electrode surface. Higher ion heights correspond to slower motional heating rates of the trapped ions [32]. However, a higher height also corresponds to a weaker trapping pseudopotential at the RF null point. The beam size of the lasers must also be considered when selecting the ion height. We describe the radius of a Gaussian beam at a distance d from the waist, $w(d)$, as follows:

$$w(d) = w_0\sqrt{1+\left(\frac{d}{d_R}\right)^2}, \quad d_R = \frac{\pi w_0^{\,2}}{\lambda} \tag{5}$$

where w_0 is the beam waist, which is the radial size of the beam at its narrowest point, and λ is the wavelength [67]. Eq. (5) indicates that a thinner beam waist can accompany a larger beam radius at the edge of the surface ion-trap chip. Figure 2-6 shows a schematic of a Gaussian beam injected parallel to the surface ion trap. An increase in the beam size induces beam clipping by the chip body, which can increase the laser scattering caused by the diffraction of the clipped laser. By setting the Rayleigh length of Gaussian beam (d_R) equal to half the traverse distance of the beam propagation above the chip as shown in Figure 2-6, the disturbance to beam propagation by the chip can be minimized. Also the ratio of ion height over beam size at the edge of the chip allows us to estimate the amount of potential laser

scattering due to laser clipping.

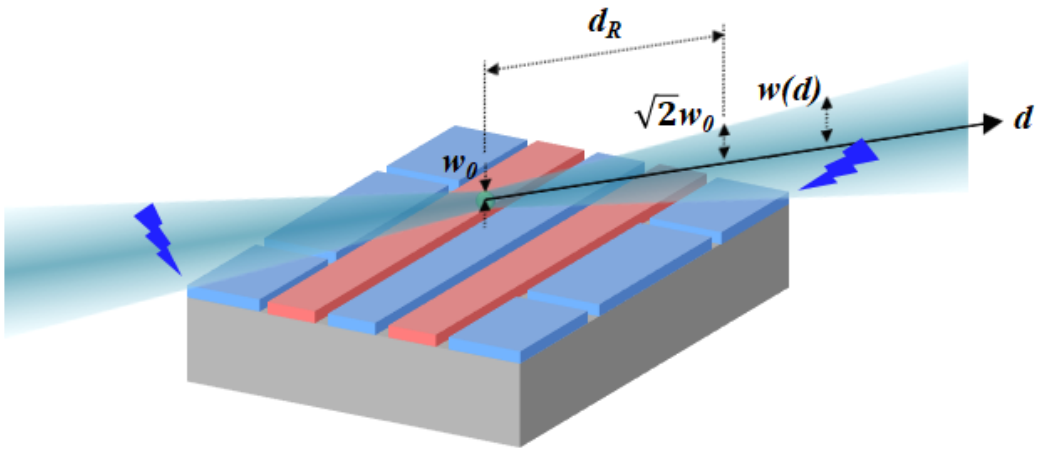


Figure 2-6. Schematic of a Gaussian beam injected parallel to the surface ion trap.

e. Analytic Solution

Based on a five-rail geometry [68], which assumes that the electrode surfaces are infinite and that there are no gaps between electrodes, the specifications of the surface ion trap described in the previous subsections are analytically solved as follows [69]:

$$\begin{aligned} \text{trap depth} &= \frac{eV^2}{m\Omega^2}\frac{(a-b)^2}{\pi^2(a+b)^2\left(a^2+6ab+b^2+4\sqrt{ab(a+b)^2}\right)} \\ \text{q-parameter} &= \frac{eV}{m\Omega^2}\frac{8(b-a)}{\pi\sqrt{ab}(a+b)^2} \\ \text{ion height} &= \sqrt{ab} \end{aligned} \tag{6}$$

where *a* and *b* are indicated in Fig. 1-6. The secular frequency can be calculated by combining Eqs. (3) and (6). However, these analytic solutions are not valid for the complex structures of actual surface ion traps, including the loading slot, finite width of outer electrodes and segmentation, and multi-layered electrodes, because certain assumptions do not hold for these complex structures. Nonetheless, these analytic solutions are very useful for making a rough first design of a surface ion trap before applying the numerical optimization procedures outlined in the following sections.

2.2.2 Simulation of Electric Potential

The application of advanced microfabrication technologies has allowed the development of complex ion trap structures such as loading slots, junctions, and even three-dimensional quadrupole structures [70]. Complex ion trap structures are difficult to be analytically modeled; therefore, simulations and numerical analyses need to be used for designing electrode dimensions of a surface ion-trap chip. We use a boundary element method (BEM) in our simulations, but finite element methods (FEM) can also be used. First, electric fields and potentials are calculated for each electrode under the assumption that 1 V is applied to that electrode while the rest of the electrodes are set to 0 V. Then the DC electric potential can be obtained by a linear combination of the individual electric potentials scaled by the actual DC voltages used. (The determination procedure for the DC voltage set is

presented in the next paragraph.) The ponderomotive potential experienced by the trapped ions is given by $\phi_{pp}(\mathbf{r}) = e|E(\mathbf{r})|^2/4m\Omega^2$, where *e, m,* Ω, $\mathbf{r}$, and $E(\mathbf{r})$ represent elementary charge, ion mass, the angular frequency of the applied RF voltage, the position vector and the amplitude of the electric field generated by the RF voltage applied to the RF electrodes, respectively. Then the total potential is simply the sum of the ponderomotive potential and the DC potential.

Figure 2-7 shows labels for the DC electrodes for the following discussion. Eight DC electrodes are grouped into outer-corner electrodes (LT, LB, RT, RB), outer-center electrodes (LC, RC), and inner electrodes (LI, RI). To utilize the reflection symmetry of the trap geometry with respect to the yz-plane at the middle of the trap, the voltages applied to each group will be decomposed into symmetric and asymmetric components. For example, we can apply a symmetric voltage V_{SO} to the outer-corner electrodes, meaning that $V_{LT} = V_{LB} = V_{SO}$ and $V_{RT} = V_{RB} = V_{SO}$. Then, the direction of the generated electric field at the middle of the trap (RF null) will be parallel to the y-axis. The amplitude of that field is $V_{SO}E_{ySO}$, where E_ySO is the amplitude when V_{SO} = 1 V. On the other hand, if we apply an asymmetric voltage V_{AO} to the same group, meaning that $V_{LT} = V_{LB} = V_{AO}$ and $V_{RT} = V_{RB} = -V_{AO}$, then the generated electric field at the RF null, $V_{AO}E_{xAO}$, will now be parallel to the x-axis. Symmetric voltages for outer-center electrodes group (V_{SC}) and for inner electrodes group (V_{SI}) can be similarly defined, which will generate $V_{SC}E_{ySC}$ and $V_{SI}E_{ySI}$ at the

RF null respectively. All these symmetric voltages will create electrical fields that are pointing in the y-direction. Similarly, asymmetric voltages for outer-center electrodes group (V_{AC}) and for inner electrodes group (V_{AI}) will generate $V_{AC}E_{xAC}$ and $V_{AI}E_{xAI}$ respectively, and they will be parallel to the x-axis. To minimize micromotion caused by non-zero DC fields at the RF null, the DC fields caused by the outer-corner electrodes group and the outer-center electrodes group must be cancelled by the DC fields generated from the inner electrodes group, namely $V_{SO}E_{ySO} + V_{SC}E_{ySC} + V_{SI}E_{ySI} = 0$ and $V_{AO}E_{xAO} + V_{AC}E_{xAC} + V_{AI}E_{xAI} = 0$.

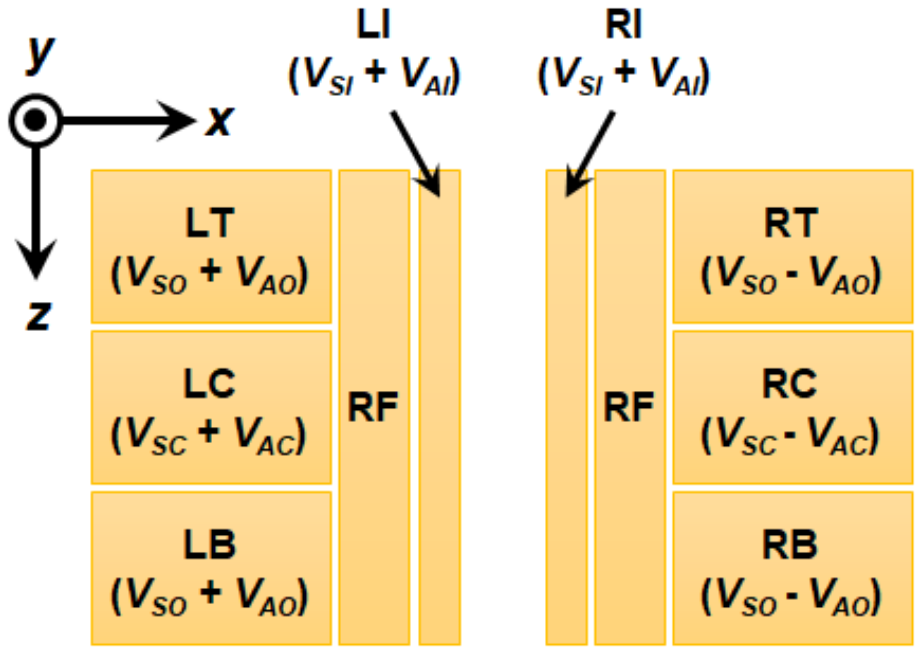


Figure 2-7. The labels used in the determination procedure of DC voltages.

For our setup, the voltages of the outer electrodes shown in Figure 4 were adopted from previous experiments using a trap chip with similar dimensions [62], and V_{SI} and V_{AI} were calculated by the method explained above. It is worth mentioning that the symmetric voltages (V_{SO}, V_{SC}) of the outer electrodes contributes heavily to the confining potential along the axial direction (z-axis), so they can be adjusted to achieve a desired secular frequency along the axial direction. For secular frequencies in the radial direction, on the other hand, one can vary the RF voltage to achieve the desired values. The asymmetric voltages (V_{AO}, V_{AC}) at the outer electrodes contribute to the tilting of the radial principal axes in the xy-plane. For optimal cooling process, tilt angle near 45 degrees is desired. During such adjustment process, output range of the DC voltage source may become the main constraint, and it is recommended that all the final voltages be at least 1 V less than the maximally allowed values so that there will always be some margin left for voltage adjustments. From the estimated total electric potential, the trap parameters described in 2.2.1.can be easily calculated. The tilted angle of the principal axes also can be obtained by computing the Hessian matrix of the total trap potential and finding the eigenvalues.

To determine the validity of the BEM tool, we simulate the electric potential generated by a simple electrode structure with 1-μm electrode gaps, as shown in the upper-left inset of Fig. 2-8. This figure shows the analytic solution from Eq. (6) and

the simulated ion heights when the segment size is 333~357 μm^2 for the RF electrodes and 6,800~7,400 μm^2 for the DC electrodes. The maximum error is 0.77% as marked with red dots and triangles in Fig. 2-8). The adaptive mesh function of the BEM tool can also be used, and the maximum error is 0.83%. Therefore, it can be concluded that the simulation results using the BEM tool seem valid for estimating the electric potentials generated by the simple trap-chip electrodes. For the case of electric potential generated by a more complex electrode configuration shown in the upper-right inset in Fig. 2-8, the analytic solutions in Eq. (6) do not valid anymore (marked with black rectangles and triangles in Fig. 2-8). In this case, the validity of the simulated values has been evaluated with the actual experimental results. With the ion-trap chip of previous version presented in 2.1.1, the secular frequencies are measured and compared with the simulated values. When applying the RF voltage of 240 V_{p-p} at the frequency of 25.4 MHz, the measured values of radial secular frequencies are 2.2 and 1.9 MHz (Fig. 2-9). The simulated values are 2.14 and 2.02 MHz, and the corresponding errors with the actual values are 2.8% and 5.9%. This results indicate that the simulation values can provide the efficient expectations for the complex ion-trap structures such as multi metal layers and loading slots.

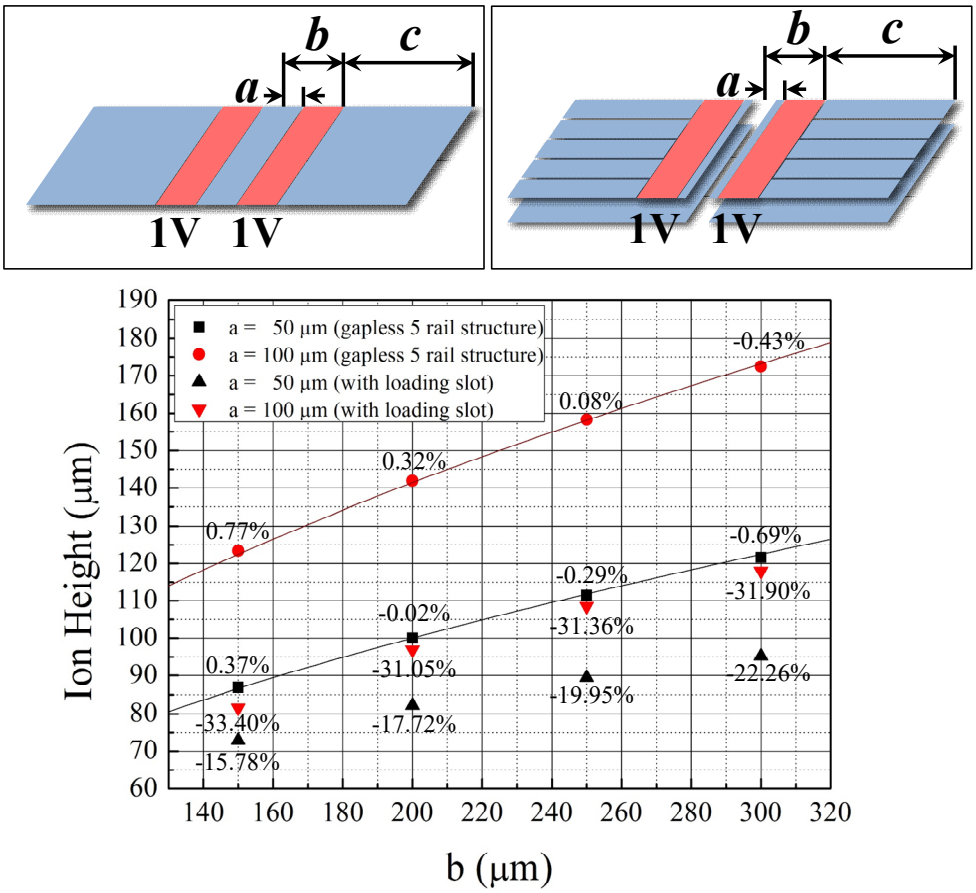


Figure 2-8. Simulation results of the ion heights for a simple electrode geometry (upper-left inset) and a complex electrode configuration (upper-right inset).

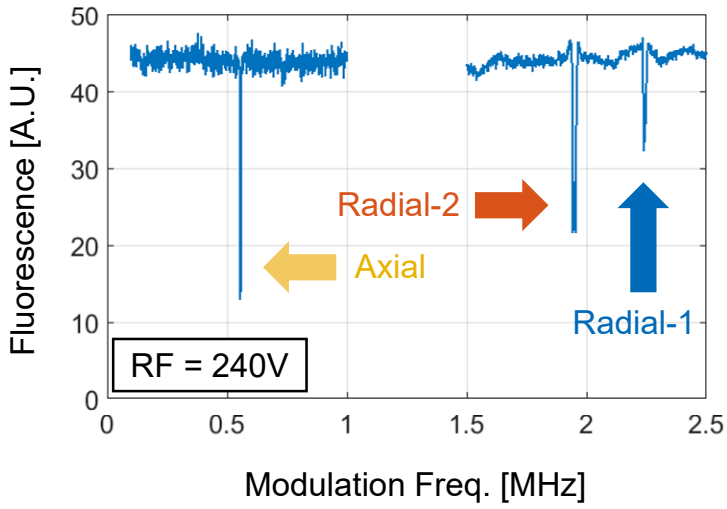


Figure 2-9. Experimental results for measuring the secular frequencies using the ion-trap chip of the previous version.

2.2.3 Electrode Dimensions and Chip Shape

a. RF Electrodes

The design of the RF electrodes is most important step in designing surface ion-trap chip, since it affects various specifications of the chip including the parameters explained in 2.2.1. To determine the dimension of the RF electrodes, the BEM simulations are performed with changing the electrode dimensions. The dimension of the RF electrodes here is represented by two parameters, *a* and *b* in Fig. 1-6. The lengths *a* and *b* determine the distance between the two RF electrodes and

the distance of the outer DC electrodes from the ion position, respectively. Between the RF electrodes, we can position a loading slot and the center DC electrodes. Thus, we determine a by the widths of the loading slot and the center DC electrodes. The width of the loading slot can be designed with respect to the configuration of the components that supply neutral atoms, and are typically tens of micrometers. The minimum value of a is determined by considering the width of the slot and the inner DC rails, which are laid between the RF electrodes. The value *b* determines the distance between the trapped ions and the DC electrodes, so the maximum value of *b* is restricted by the effects of the DC voltages at the ion position. The constraint dimensions are initially established by referring to previous work and must be optimized by repetitively designing the RF electrodes and DC voltage set.

Table 1 shows the simulation results according to the dimensions of the RF electrodes. The input intervals of 10 μm is used in the simulations. The ytterbium ion is considered to be used, and the amplitude and the frequency of the RF voltage is assumed as 300 V and 50 Ω in the simulation sets, respectively. One of the noteworthy parameters is (trap depth) / (q-parameter). According to Equation (6), the trap depth, radial secular frequencies, and q-parameter are proportional to V^2/Ω^2, V/Ω, and V/Ω^2, respectively. It means that the trap depth and the q-parameter can be adjusted in the same proportion. Thus, the higher (trap depth) / (q-parameter) value allows the deeper trap depth when considering the same q-parameter.

a (μm)	b (μm)	150	160	170	180	190	200	210	220	230	240	250
40	Trap depth	0.3482	0.3402	0.3316	0.3204	0.3120	0.3036	0.2938	0.2861	0.2786	0.2701	0.2632
	q parameter	0.2770	0.2652	0.2540	0.2421	0.2323	0.2242	0.2151	0.2075	0.2010	0.1940	0.1880
	Trap depth / q	1.257	1.283	1.305	1.323	1.343	1.354	1.366	1.378	1.386	1.392	1.400
	Ion height	55.74	57.41	59.01	60.75	62.17	63.52	65.01	66.24	67.39	68.69	69.74
50	Trap depth	0.2493	0.2446	0.2421	0.2388	0.2332	0.2293	0.2251	0.2196	0.2153	0.2110	0.2057
	q parameter	0.2112	0.2020	0.1952	0.1885	0.1812	0.1754	0.1698	0.1640	0.1594	0.1547	0.1500
	Trap depth / q	1.180	1.211	1.240	1.267	1.287	1.308	1.326	1.339	1.351	1.364	1.371
	Ion height	61.41	63.62	65.46	67.21	69.09	70.65	72.15	73.75	75.11	76.40	77.80
60	Trap depth	0.1798	0.1816	0.1802	0.1802	0.1793	0.1766	0.1749	0.1729	0.1697	0.1673	0.1648
	q parameter	0.1631	0.1589	0.1536	0.1496	0.1454	0.1407	0.1371	0.1335	0.1298	0.1264	0.1232
	Trap depth / q	1.102	1.143	1.173	1.205	1.233	1.255	1.276	1.295	1.308	1.324	1.338
	Ion height	65.77	68.00	70.35	72.32	74.20	76.19	77.86	79.48	81.19	82.65	84.05

Table 1. Simulation results for different electrode dimensions.

The selection of the electrode dimension is a trade-off problem among various trap parameters, and the priorities of the parameters can be assigned according to the experimental goal. The chip in this dissertation will be used in the experiments for investigating the effects of the dielectric charging. In the experiments, the distance of the axial shift of the trapped ion induced by the stray fields which are intentionally generated is measured. Therefore, the goal of this design procedure is to maximize the trap depth which means the strong confinement in the radial direction, to prevent the escape of the trapped ion under the induced stray fields. The q-parameter is fixed at a constant value of 0.25. By considering this conditions, the dimensions of a = 40 μm and b = 200 μm is selected. To obtain the deep trap depth, the relatively low height of the ion and effects of DC voltages can be borne. Note that this dimension is not an optimized one but an appropriate compromise solution. The simulated parameters corresponding to the dimensions are trap depth of 0.329 eV, the q-parameter of 0.242, the radial frequencies of 4.0 MHz, the axial frequency of 304 kHz, the ion height of 60 μm, and the tilted angle of the principal axes is 47 degrees.

b. Overall Chip Shape

After designing the dimensions of the RF electrodes, the size and shape of the chip should be designed. As shown in Eq. (5), the beam radius increases with

distance from the waist. Therefore, a smaller chip size is advantageous for preventing laser clipping at the chip edges. One of the factors that restrict the chip miniaturization is the size and number of the DC electrodes. Also, the distance from the wire bonding pads on the chip to the corresponding pins on the chip carrier must not exceed the length limit of the wire bonding process. In this dissertation, the suppression of the beam scattering is tried by minimizing the lengths of the chip along the considered beam directions. The design considers the beam paths along the off-diagonal and the horizontal directions as shown in Fig. 2-10. The widths of the chip along the off-diagonal and the horizontal directions are 2.26 mm and 2.5 mm, respectively. Figure 2-11 shows the proportion of the clipped beam power as a function of ion height when the laser wavelength of 369.5 nm and the distance between the chip center and the edge is 2.26 mm. The disturbance to beam propagation by the chip body is minimized when the beam waist is equal to $(l\lambda/\pi)^{1/2}$, where l is the distance between the waist and the chip edge where beam clipping occurs, and the proportion of the clipped beam is minimized when the beam waist is 16.32 μm in this case. The proportion of the clipped beam power is 10^{-5} for the beam waist of 16.32 μm and the ion height of 60 μm, and seems sufficiently low.

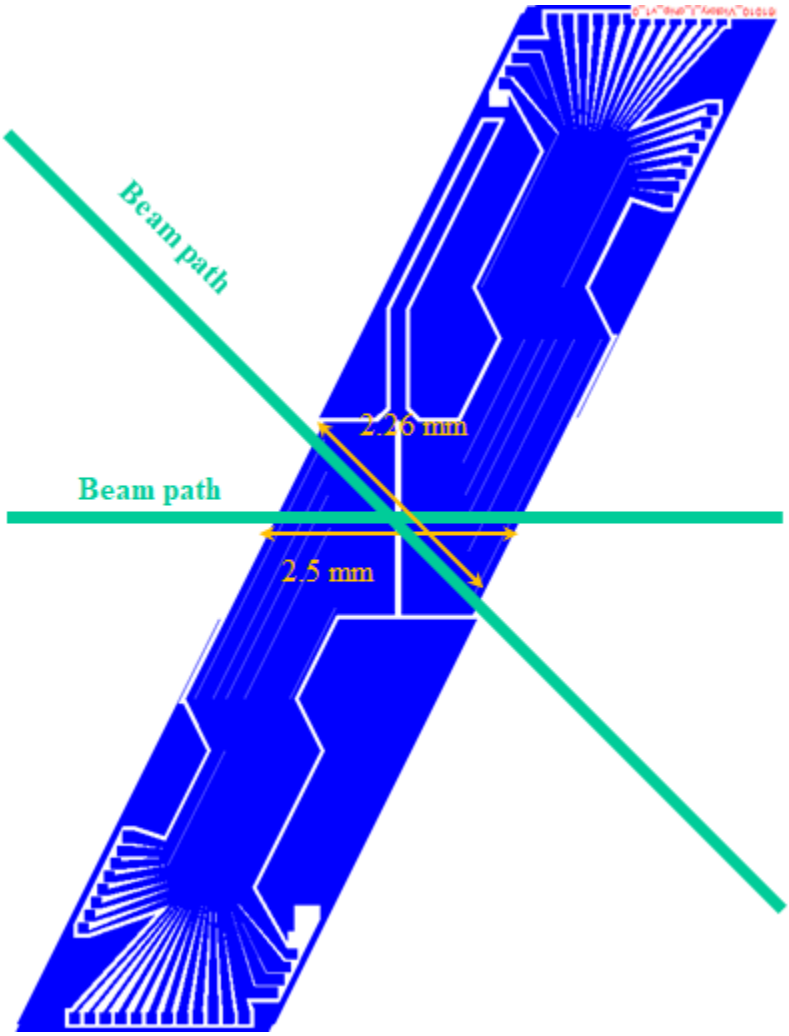


Figure 2-10. Overall chip shape and the considered beam path.

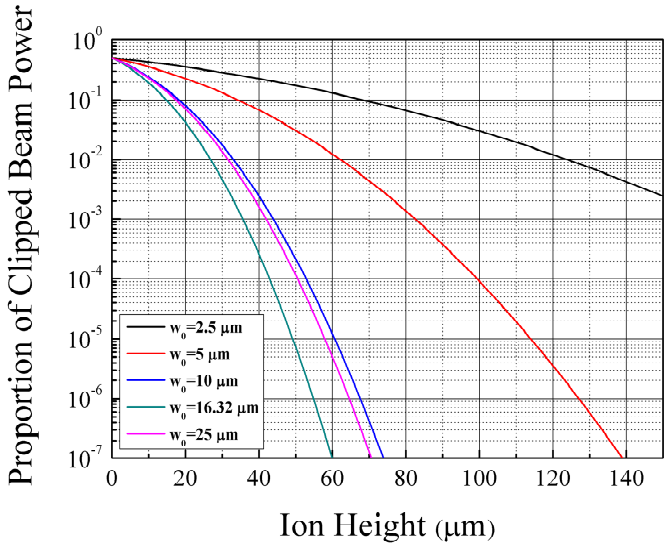


Figure 2-11. Proportion of the clipped beam power as a function of ion height.

The number and width of the segmented DC electrodes defines the length of the RF rails and the trapping region. The number of the DC electrodes also determines the required lateral spaces for wiring the DC electrodes to the wire bonding pads which are assigned at the edge of the chip and the number of required bonding pads. Therefore, the design of the DC electrodes should be compatible with the designed chip shape and the considered chip carrier. Figure 2-12 shows the magnified view of the outer DC electrodes. The width of the DC electrode near the trapping region is designed to be 70 μm by referring the previous researches [44, 56]. The width is decreased to be 20 μm at the region apart from the chip center, to reduce the required area for wiring the DC electrodes. The 24 pairs of the DC

electrodes can be laid on the designed chip shape with those electrode dimensions. Figure 2-13 illustrates the schematic of the ion-trap chip mounted on the chip carrier and the bonding wires. The chip is assumed to be mounted on the commercial chip package (IPKX0F1-8180BA, NTK Ceramic, Co. Ltd.) with a mounting area of 1.2 cm × 1.2 cm. The chip carrier has a total pin number of 100, but nearly a half of the pins cannot be used not to interfere the beam propagation.

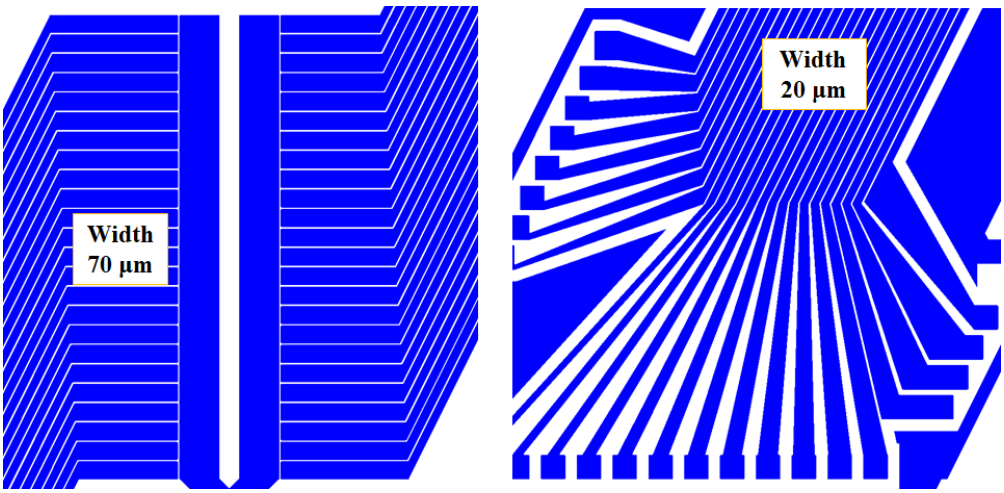


Figure 2-11. Magnified view of the outer DC electrodes.

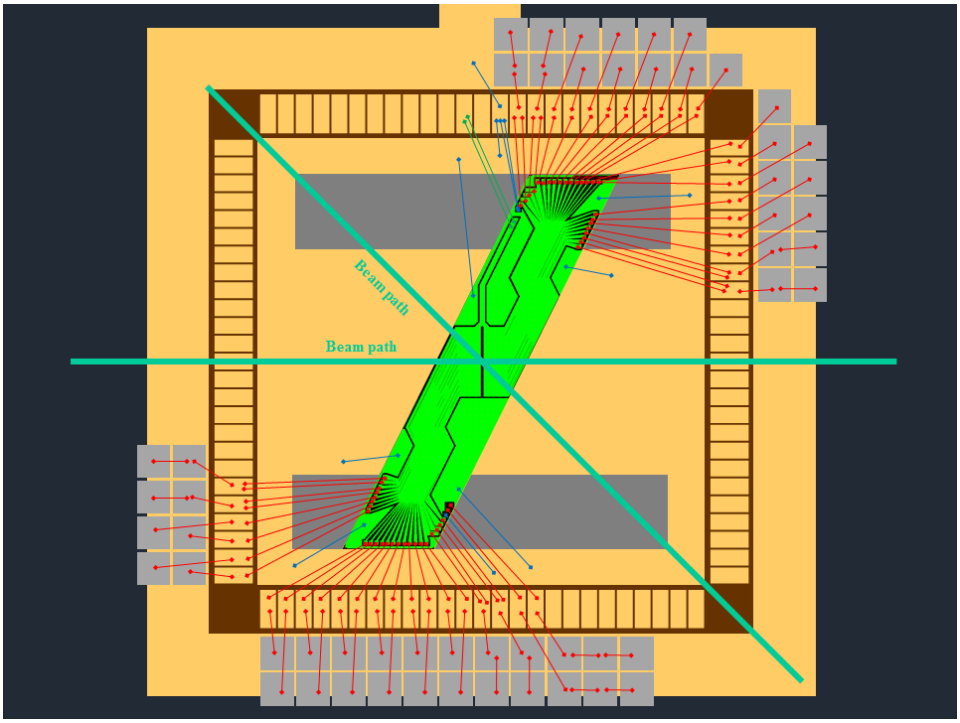


Figure 2-13. Wire bonding diagram for the proposed chip.

c. Mask Layout

Based on the design procedure described above, the mask layout is designed. The total layout includes 9 mask layers. The first layer defines a metal contact on the silicon substrate which makes the direct wire bonding to the silicon substrate easier. The second, the fifth, and the sixth layer are for patterning the ground plane, the inner DC rails, and the loading slot and share some overlapped patterns. The third layer is to carve dummy patterns on the I2 layer, and the patterns are used to measure the thickness of the chemical mechanical polishing (CMP) process. The

fourth, the eighth, and the ninth layers are for fabricating the oxide pillars and the electrodes. The patterns in the fourth layer which define the lower part of the oxide pillars are 8 μm larger than those in the eighth layer for etching the upper part of the pillars, as mentioned in the 2.1.2. The ninth mask layer is for defining the top electrode layer and 2 μm larger than the eighth layer by considering the align margin of the photolithography process. The resolution of the mask aligner (MA6, Karl-Suss) is about 0.7 μm in the best conditions, but normally about 1.6 μm. Figures 2-14 shows the magnified images of the mask layouts.

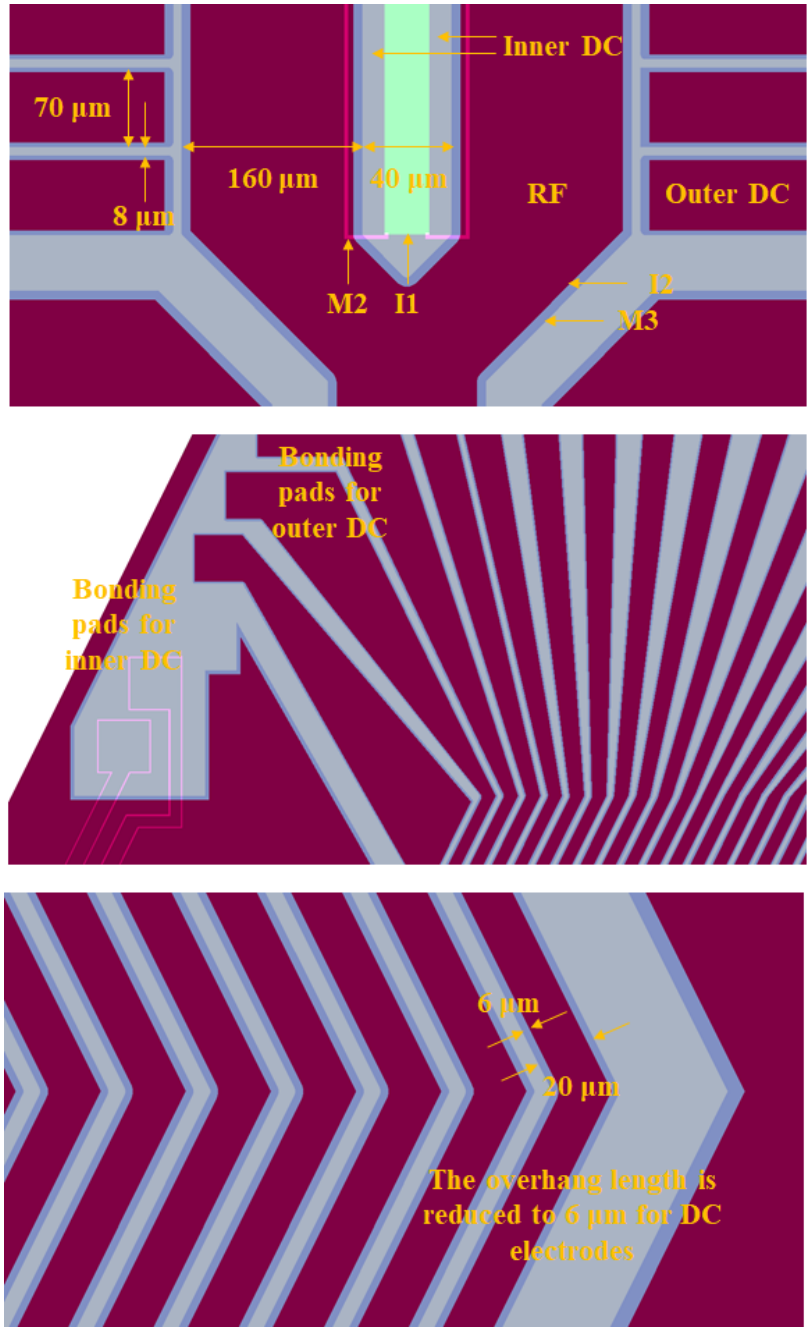


Figure 2-14. Magnified images of the mask layout.

Chapter 3

FABRICATION

3.1 Material and Equipment

A sacrificial process need be used to fabricate the overhang structures of the dielectric pillars. The sacrificial material should be determined by considering the feasibility of selective removal and the sufficiently high rigidity not to cause dishing during a CMP process. In addition to them, the thermal budget of the entire process should also be regarded, since the I2 layer with the thickness of 4 μm is deposited by a plasma enhanced chemical vapor deposition (PECVD) process at 350°C, after the sacrificial layer is formed. Figure 3-1 shows an example of the failures, a crack in oxide pillars, which indicates that the residual stress accumulated in the sacrificial layer during the cool-down step after the high-temperature deposition process can

damage the structural layer. Considering these requirements, a cured polyimide (PI-540, ACT corp.) is used for the sacrificial material in this fabrication process.

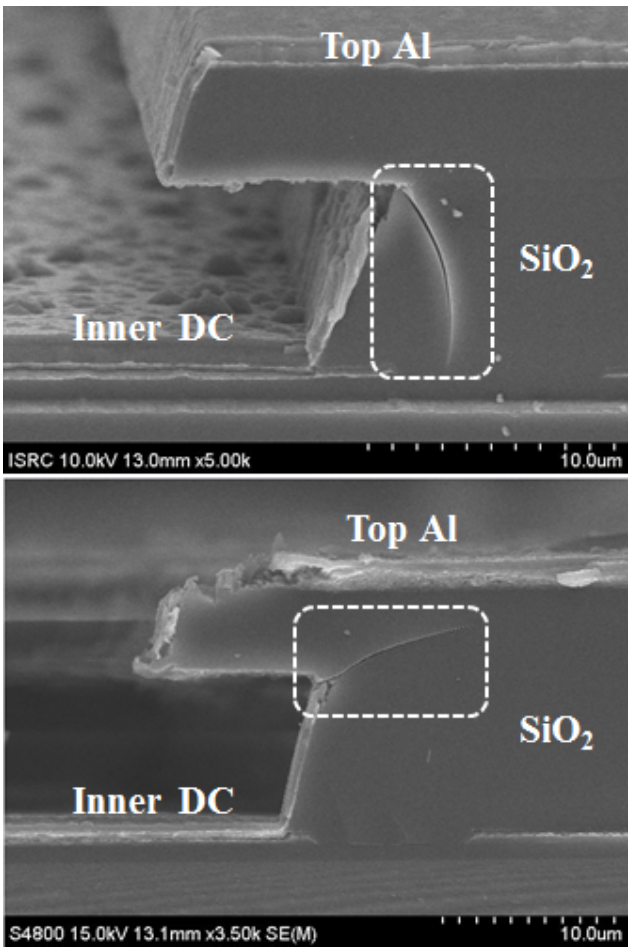


Figure 3-1. Two different types of the cracks in the oxide pillar.

The metallic materials used in this dissertation are aluminum, gold, and titanium. All of them are deposited by sputtering processes. The aluminum alloy contains 1% copper to prevent whisker formations during the baking process to reach a UHV environment. This composition is essential for whisker prevention. The process parameters for the Al sputtering process (MHS-1500, Muhan Vacuum) are: Ar flow rate of 40 sccm, pressure of 2 mTorr, and RF power of 300 W, which result in a deposition rate of 130 Å/minute. The process parameters for the Au and Ti sputtering (ALPS-C03, Alpha-Plus) are: Ar flow rate of 40 sccm, pressure of 5 mTorr, and DC power of 500 W, which result in a deposition rate of 130 Å/minute. The aluminum layer is dry-etched by an inductive coupled plasma (ICP) type etcher (PlasmaPro System100 Cobra, Oxford Instrument). An ICP etcher was used with the following process parameters: BCl_3 flow rate of 20 sccm, Cl_2 flow rate of 30 sccm, pressure of 5 mTorr, and RF power of 750 W, which result in an etch rate of 3600 Å/minute.

For the insulating layer, PECVD SiO_2 is used. The process parameters used in the PECVD process (PlasmaPro System 100, Oxford Instrument) are: SiH_4 flow rate of 540 sccm, pressure of 1.9 Torr, process temperature of 350°C, and RF power of 750 W, which result in a deposition rate of 3000 Å/minute. To dry-etch the SiO_2 films, a reactive ion etching (RIE) process is used (P-5000, Applied Materials). The process parameters for SiO_2 etching were: CHF_3 flow rate of 25 sccm, CF_4 flow rate

of 5 sccm, Ar flow rate of 50 sccm, pressure of 130 mTorr, and RF power of 600 W, which result in an etch rate of 3600 Å/minute. As mentioned before, boron-doped single crystalline silicon is used as the substrate. The silicon should be penetrated to provide a loading slot by using a deep reactive ion etching (DRIE) process (SLR-770-10R-B, Plasma-Therm). The DRIE process was performed with the iterations of C_4F_8 deposition for 5 seconds, C_4F_8 etch for 3 seconds, and Si etch for 5 seconds. In the C_4F_8 deposition step, the flow rates of C_4F_8, SF_6, and Ar were 100, 0.5, and 30 sccm, respectively. In the C_4F_8 etch step, the flow rates were changed to 0.5, 50, and 30 sccm, respectively. In the Si etch step, the flow rates of 0.5, 100, and 30 sccm, respectively, were used. The RF power and the chamber pressure were set to 825 W and 23 mTorr in all steps. For these conditions, the etch rate of the Si was 1 μm for each loop.

Two types of photoresists (PR) are used in the process. The first one is AZ7220 (AZ materials) whose target thickness is approximately 2 μm. The process parameters for this PR are: spin speed of 5000 rpm, spin time of 40 seconds, pre-bake temperature of 95°C, pre-bake time of 90 seconds, exposure energy of 144 mJ/cm^2, develop time of 60 seconds, post-bake temperature of 110°C, and post-bake time of 5 minutes. The second one is AZ4620 (AZ materials) whose target thickness is approximately 6 μm. The process parameters for this PR are: spin speed of 5000 rpm, spin time of 40 seconds, pre-bake temperature of 95°C, pre-bake time of 5

minutes, exposure energy of 900 mJ/cm^2, develop time of 10 minutes, post-bake temperature of 110°C, and post-bake time of 5 minutes. To remove these PR after being used as the etching mask, a O_2 plasma asher (300Semi-Autou, Tepla AG.) The process parameter for the ashing process are: power of 700 W and O_2 flow rate of 700 ml/min.

3.2 Aluminum Trap

3.2.1 Fabrication Process

The fabrication process of proposed ion-trap chip is following. A silicon wafer is prepared and cleaned with piranha solution (H_2SO_4:NH_4F=4:1) for 20 minute at 180°C. A 0.4-μm thick Al layer is deposited on the silicon substrate. A 2-μm thick PR is coated and patterned to define the aluminum contact pad for connecting bonding wires on the silicon substrate. The aluminum layer is wet-etched for 12-15 minutes by a mixed aluminum etchant (H_3PO_4:HNO_3:CH_3COOH:H_2O = 16:1:1:2). The wet-etching is preferred in this step, since the light field in the photomask is too wide. The used photoresist is removed with an O_2 plasma ashing process. A 1-μm thick SiO_2 (I1) layer is deposited to electrically isolate the silicon substrate and the ground plane (Fig. 3-2(a)). A 0.8-μm thick Al (M1) layer is deposited on the I1 layer. A 2-μm thick PR is coated and patterned to define the gaps between the ground

plane and the inner DC rails which will be buried under the oxide pillars. The M1 layer is dry-etched, and the used PR is removed (Fig. 3-2(b)). A 10-μm thick SiO_2 (I2) layer is deposited on the both side of the wafer. During deposition of the thick dielectric layer, the residual stress from deposited films can cause bowing of the substrate or damages to the deposited films. Thus, controlling the residual stress is one of the key techniques in the fabrication of the surface ion traps. In this process, 2.5-μm-thick SiO_2 films were deposited alternatingly on both sides of the wafer for four times, to reduce the effects of accumulated stress. A 2-μm thick PR is coated and patterned to present the dummy patterns which are used to measure the polished depth during the CMP process. Using this PR as an etching mask, the I2 layer is dry-etched for 1 μm. The used PR is removed. Note that this step and the dummy pattern are not illustrated in the schematics of the fabrication process. A 2-μm thick PR is coated and patterned to define the lower part of the oxide pillars. The I2 layer is dry-etched again, and the pillars are formed (Fig. 3-2(c)). The profile of these oxide pillars is approximately 75 degrees to allow the deposition of a metal layer on the sidewalls of the pillars. After the dry-etching of the oxide pillars, the used PR cannot be easily removed only with the O_2 plasma treatment, then the wafer can be dipped into a heated PR remover (PRS-2000, J. T. Baker) or sonicated before ashing. An additional 0.8-μm thick Al (M2) layer is deposited on the sidewalls of the pillars as well as the top surfaces. A 6-μm thick PR is coated and patterned to define the inner

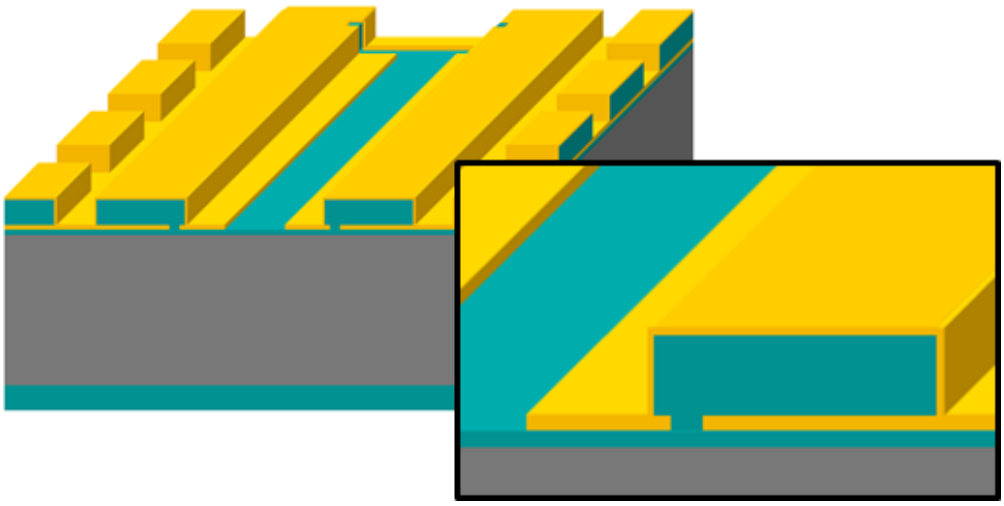
DC rails and the loading slot. Patterning the PR coated on the sidewalls of the pillars requires additional exposure and development time, and the time is extended for 30%. The aluminum layer on the sidewalls of the pillars is dry-etched, and an additional aluminum wet-etching is following to cleanly etch the residual aluminum on the sidewalls (Fig. 3-2(d)). The used PR is removed by an ashing process. A 6-μm thick PR is coated and patterned to reveal the silicon substrate between the inner DC electrodes and define the loading slot. The I1 layer is dry-etched by using the patterned PR as an etching mask, and the used PR is removed (Fig. 3-2(e)). A polyimide layer is spin-coated on the pillar structures and cured at 300°C for 2 hours. The fabricated structures are planarized by a CMP process (Fig. 3-2(f)). After the CMP process, the thickness of the oxide pillars is approximately 8 μm, and the polyimide layer filled the gaps between the pillars. A 4-μm thick SiO_2 layer is deposited on the both sides of the wafer. The SiO_2 layer deposited on the back side with the total thickness of 14 μm is dry-etched to provide a hard mask for backside DRIE process (Fig. 3-2(g)). A 6-um thick PR is used as the etching mask in this step and removed after patterning. A 0.3-μm thick aluminum layer is sputtered on the front of the wafer. This layer is dry-etched with the 2-um thick PR and used as a hard mask for dry-etching the I3 layer. The used PR is removed, and the I3 layer is dry-etched (Fig. 3-2(h)). A 1.5-μm thick Al (M3) layer is sputtered and dry-etched by using a 6-μm thick PR as an etching mask to provide the RF rails and the

segmented DC electrodes (Fig. 3-2(i)). Then, the silicon wafer is etched from the back of the wafer by a DRIE process, and the etch depth is 470 μm (Fig. 3-2(j)). After the DRIE process, the wafer is diced into pieces. Die-level processes include the removal of the polyimide sacrificial layer to release the overhang structure of the oxide pillars by using a photoresist remover and O_2 plasma ashing process (Fig. 3-2(k)), and the penetration of the loading slot by a DRIE process from the front of the wafer (Fig. 3-2(l)). Now, the fabrication of the ion-trap chip with the aluminum electrodes are finished.

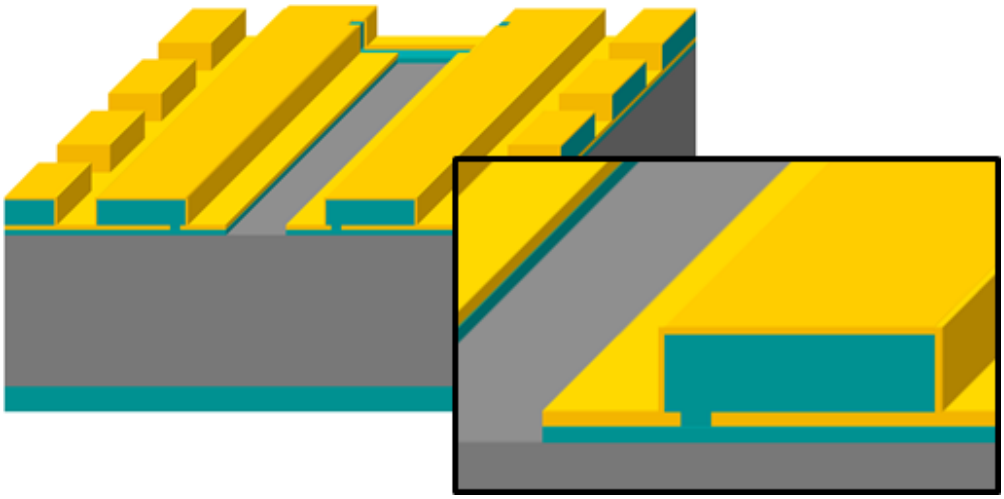
(a) SiO_2 deposition (I1)

(b) Al deposition and patterning (M1)

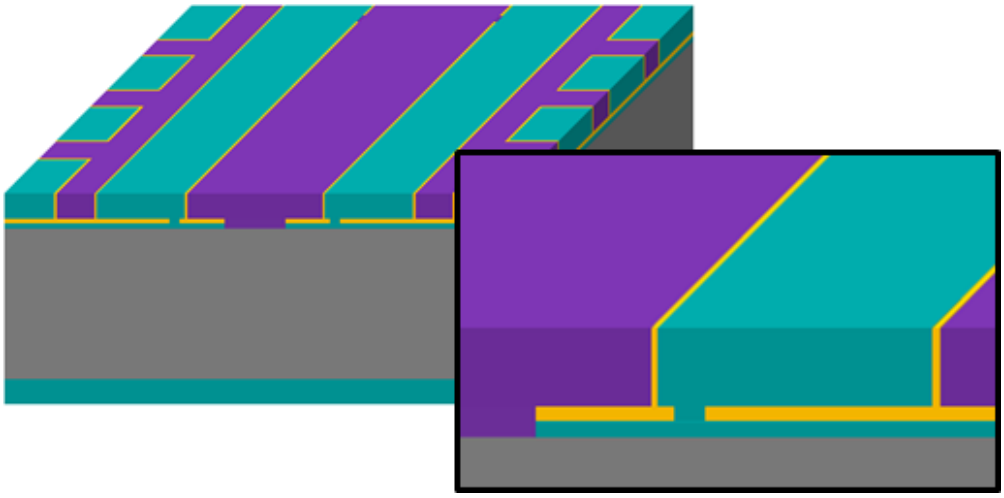
(c) SiO_2 deposition and patterning (I2)



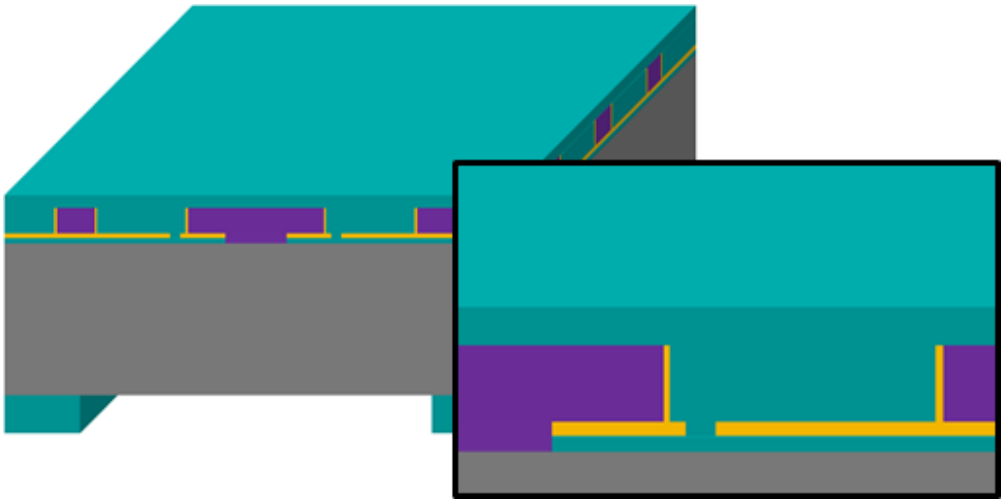
(d) Al deposition and patterning (M2)



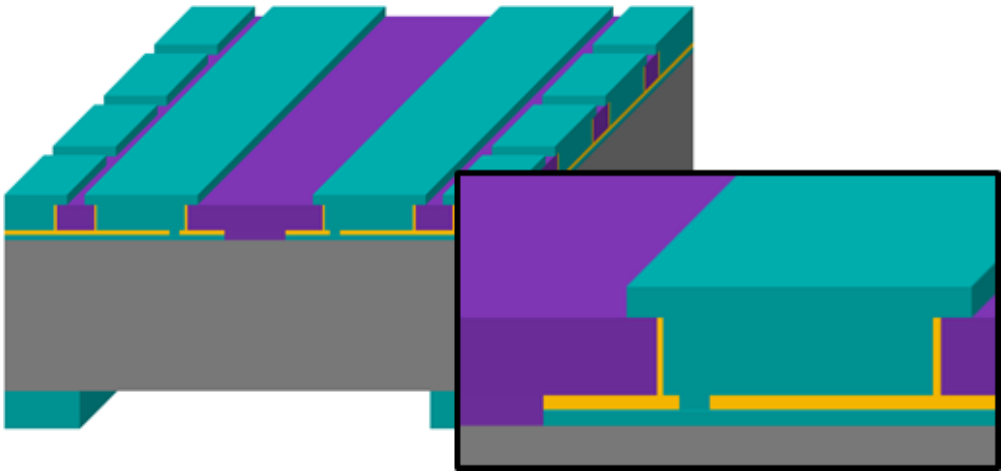
(e) SiO_2 patterning (I1)



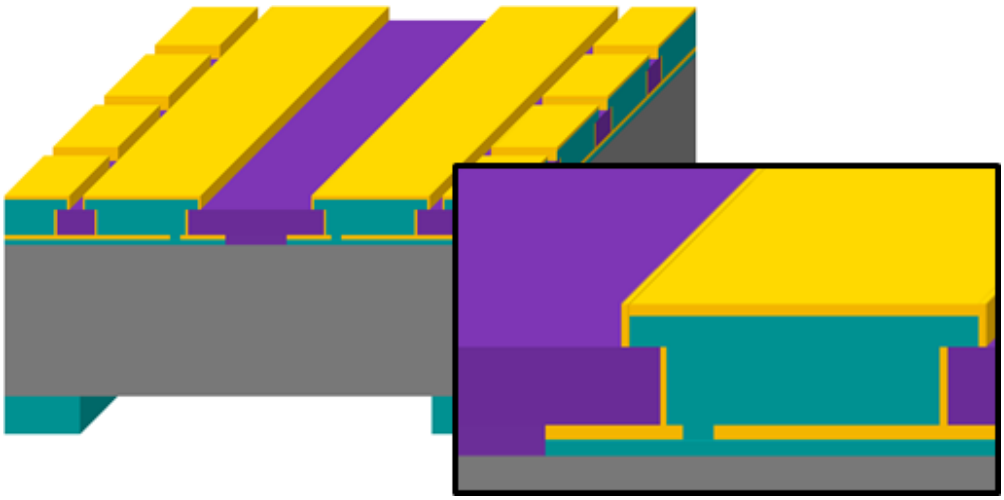
(f) Polyimide coating and CMP



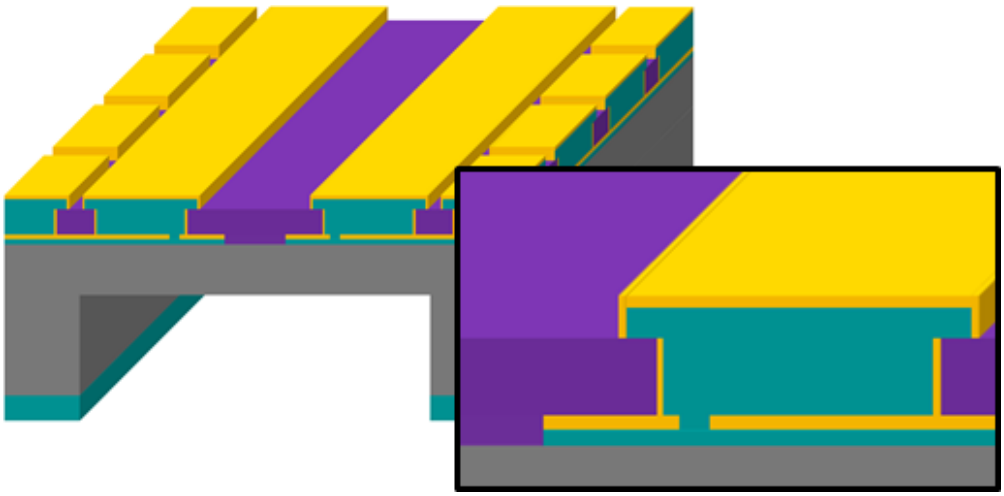
(g) SiO_2 deposition and patterning (backside)



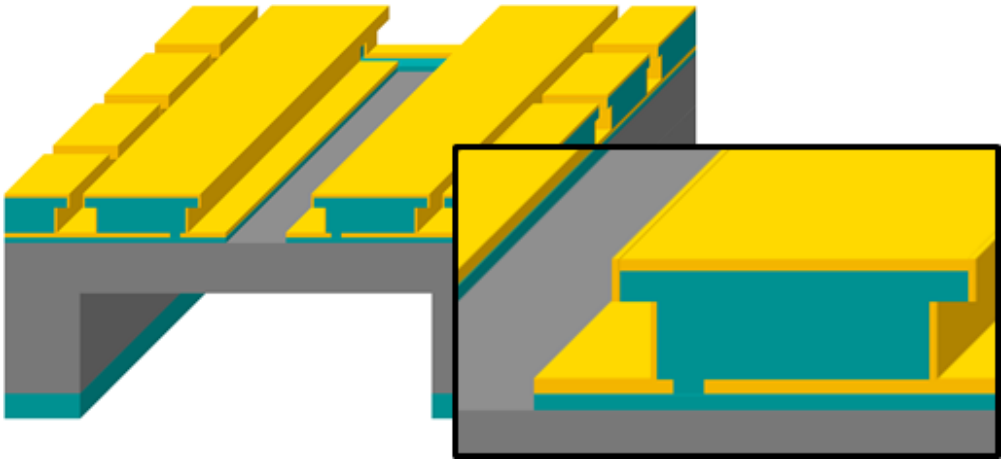
(h) SiO2 patterning (I3)



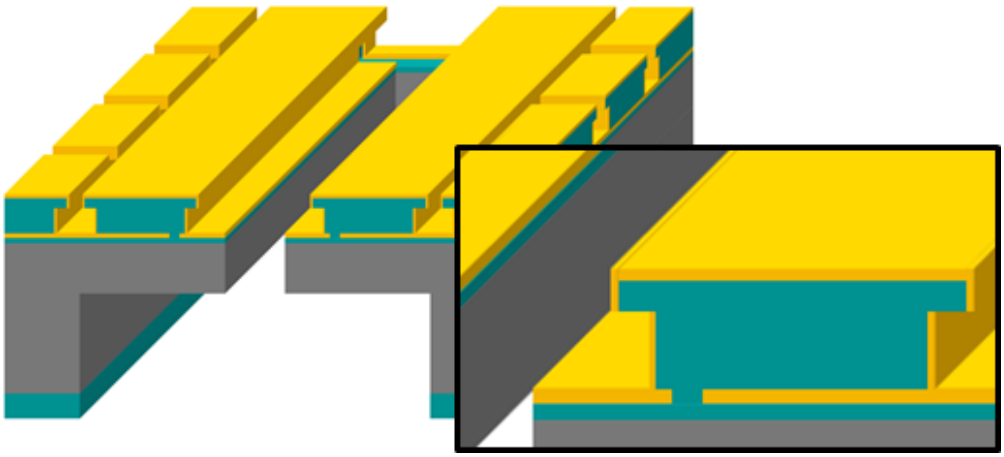
(i) Al deposition and patterning (M3)



(j) DRIE (backside)



(k) Polyimide removal



(l) DRIE (frontside)

Figure 3-2. Fabrication process flow of the proposed method.

3.2.2 Fabrication Result

Figure 3-3 show the optical image of the fabricated trap chip with aluminum electrodes. Note that this figure is a mosaic of the optical images. Scanning electron micrograph (SEM) images show the fabricated structures more clearly. Figure 3-4(a) shows the overall shape of the chip. The magnified images taken from the top are shown in Figures 3-4(b)-3-4(d). Figure 3-4(b) shows the trapping region including the RF electrodes, the inner DC electrodes, the segmented DC electrodes, and the loading slot. Figure 3-4(c) shows the wire bonding pads for the inner DC electrodes, which are wired to the edge of the chip through the M1 layer buried under the oxide

pillars. Figure 3-4(d) shows the segmented DC electrodes whose widths are 20 μm. Figure 3-5(a) shows a cross-sectional image near the loading slot, and Figures 3-5(b), 3-5(c) show the magnified view of Figure 3-5(a). The distances between the isolated electrodes are larger than 8 μm through vacuum space, and larger than 4 μm through SiO_2. Entire protection of the sidewalls of the RF electrodes facing to each other indicates that no misalignment occurs during the photolithography process for patterning M3 layer. The lower and the upper parts of the dielectric pillars are coated by separate aluminum films. Also, Figs. 3-5(b) and 3-5(c) show that the depth of dishing that arises in the CMP step is sufficiently shallow to be ignored. Figure 3-5(d) is similar to Fig. 3-5(c), but colored for clarity. Figure 3-5(e) shows a cross-sectional view showing the gap between the RF and DC electrodes. Both the facing sidewalls are successfully coated by aluminum films. Figure 3-5(f) is a tilted view of the segmented DC electrodes. It is shown that no dielectric surfaces are revealed to this sight.

The electrical connections among the electrodes and the ground plane is inspected by probing directly on the chip. At the early stage of process development, an electrical short between the inner DC rail and the ground plane occasionally occurs because of the failure in the sidewall patterning. However, the addition of the wet etching process to the sidewall patterning step can eliminate this problem.

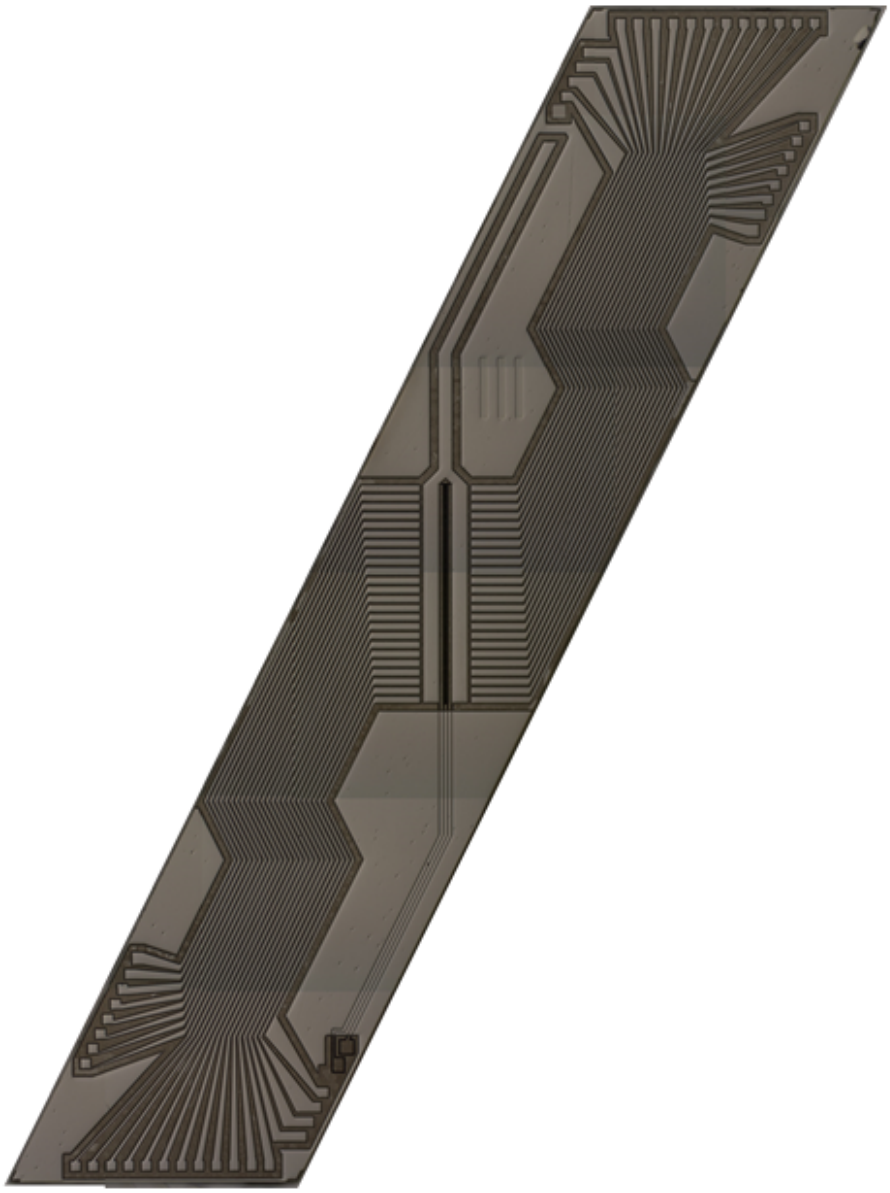
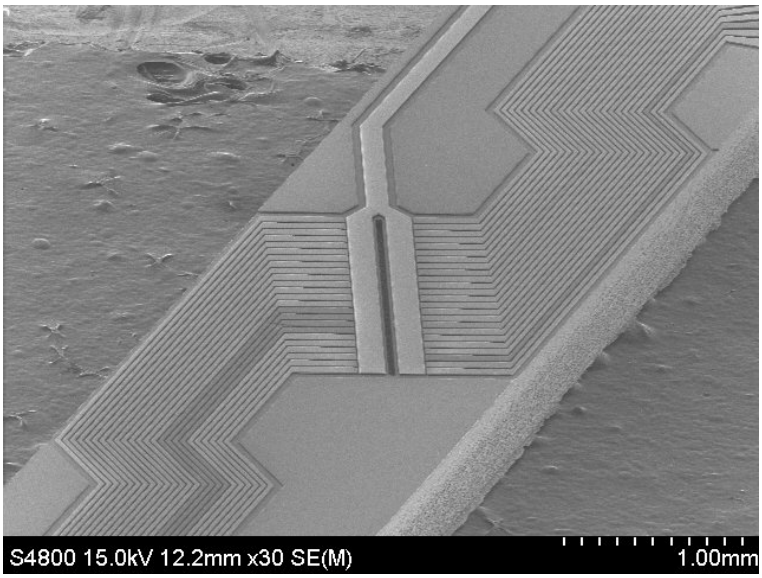
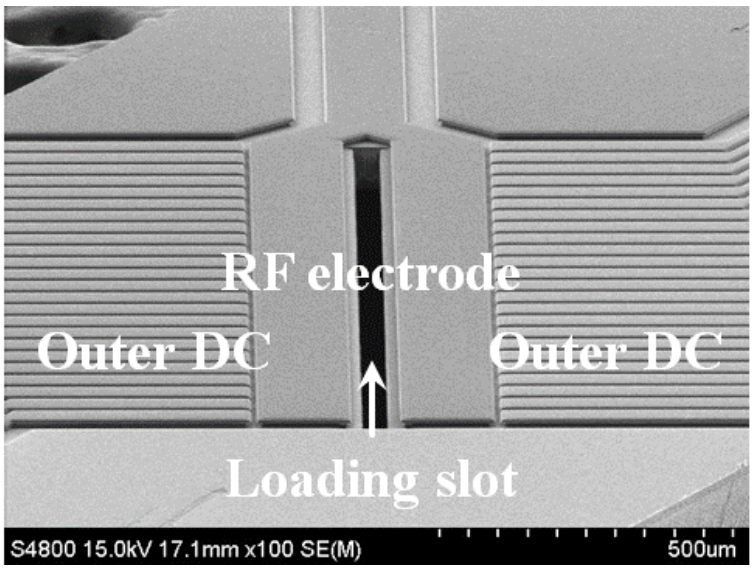


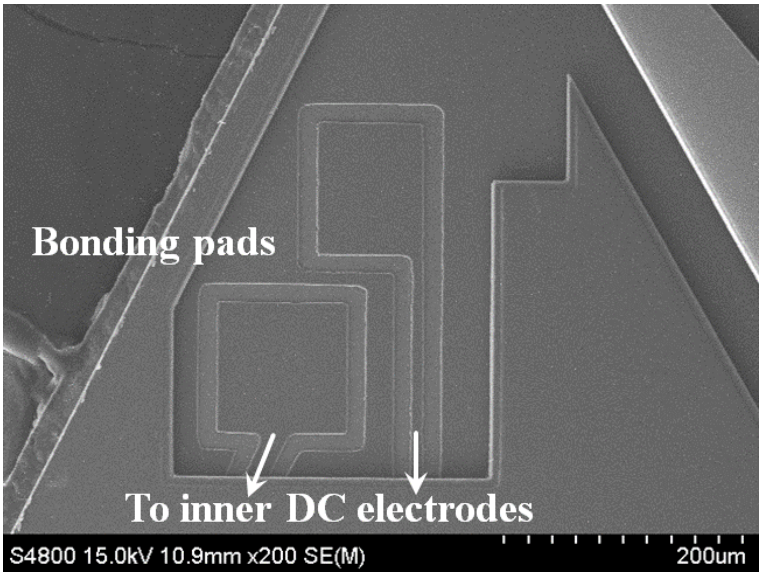
Figure 3-3. Mosaic optical image of the ion-trap chip with aluminum electrodes.



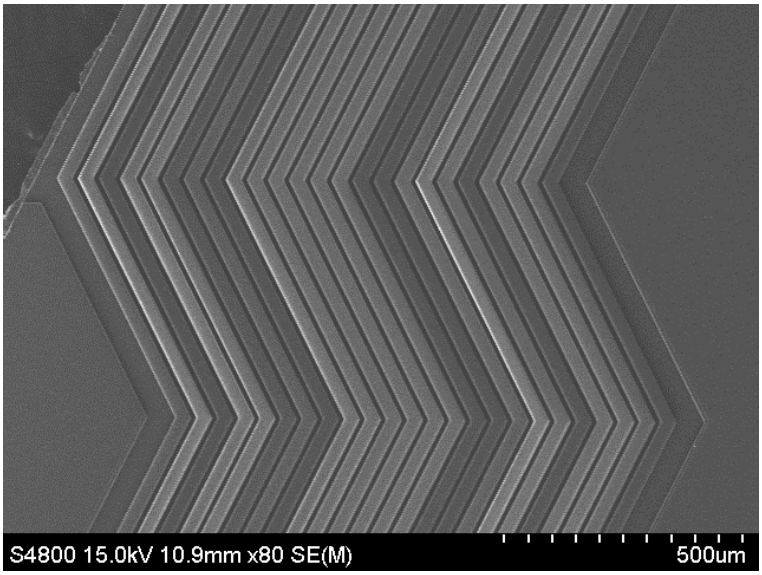
(a) Overview of the chip



(b) Magnified view showing the trapping region

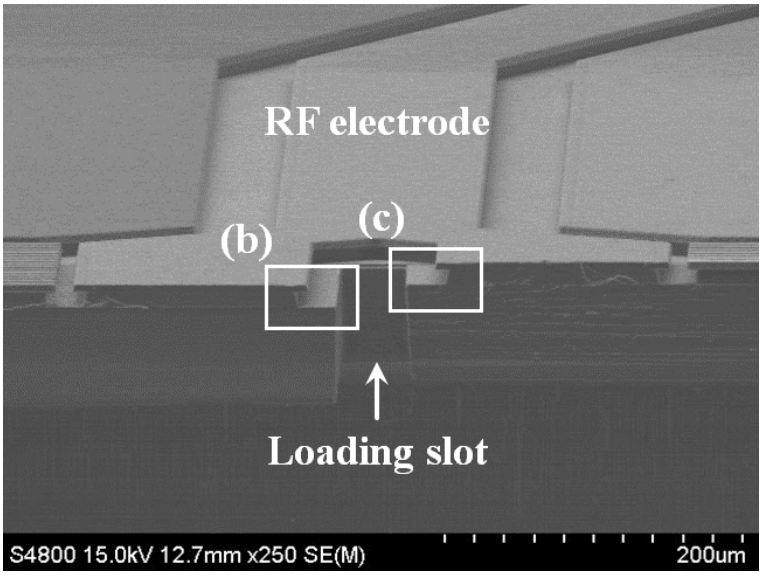


(c) Bonding pads of the inner DC rails

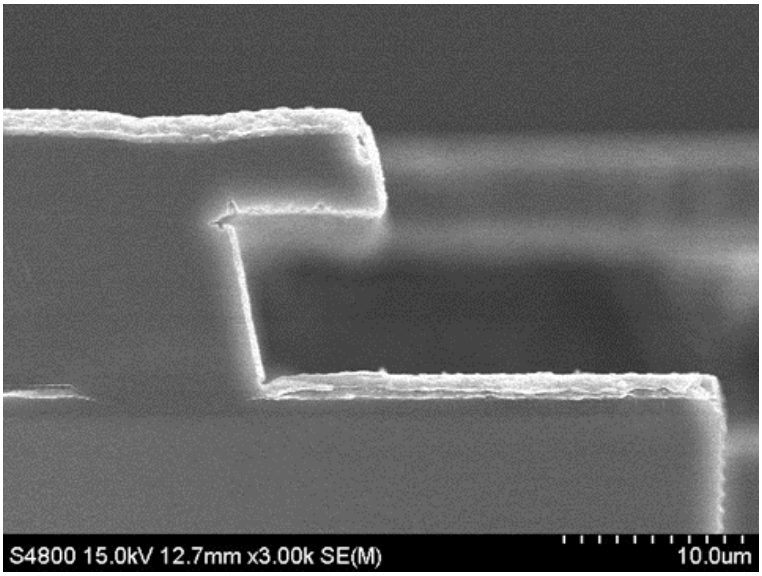


(d) Segmented DC electrodes

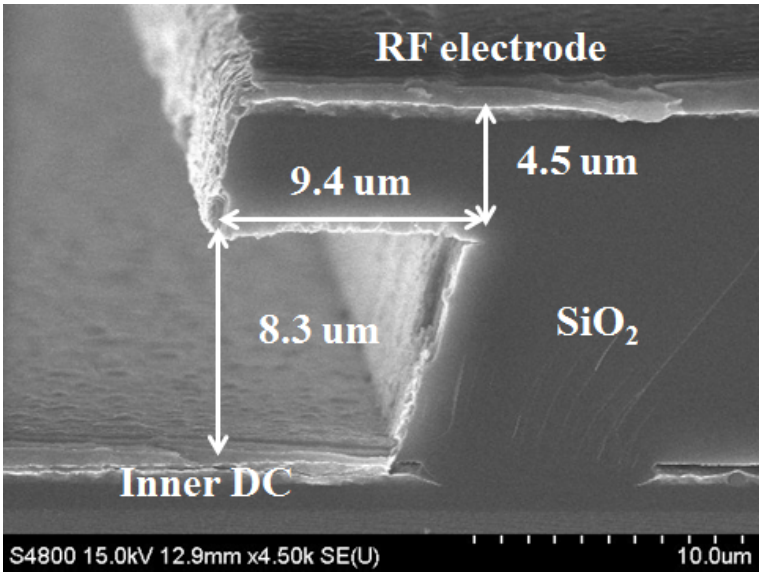
Figure 3-4. Top-view SEM images of the trap chip with aluminum electrodes.



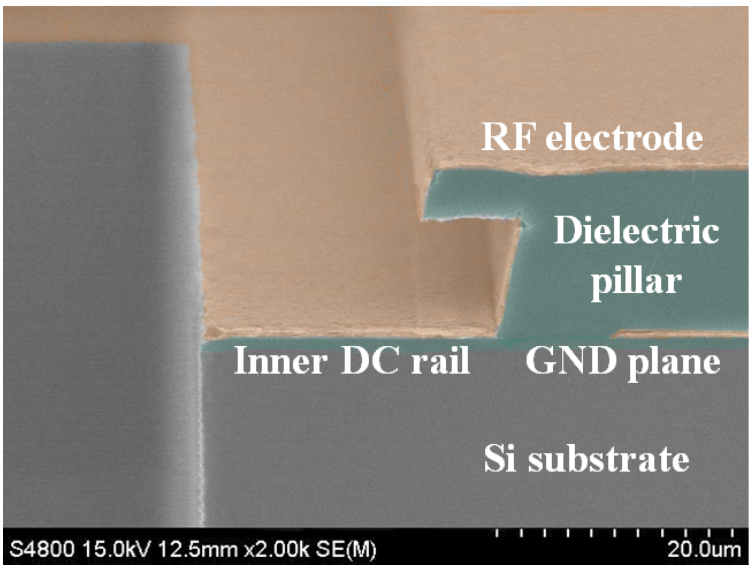
(a) Overview of the loading slot



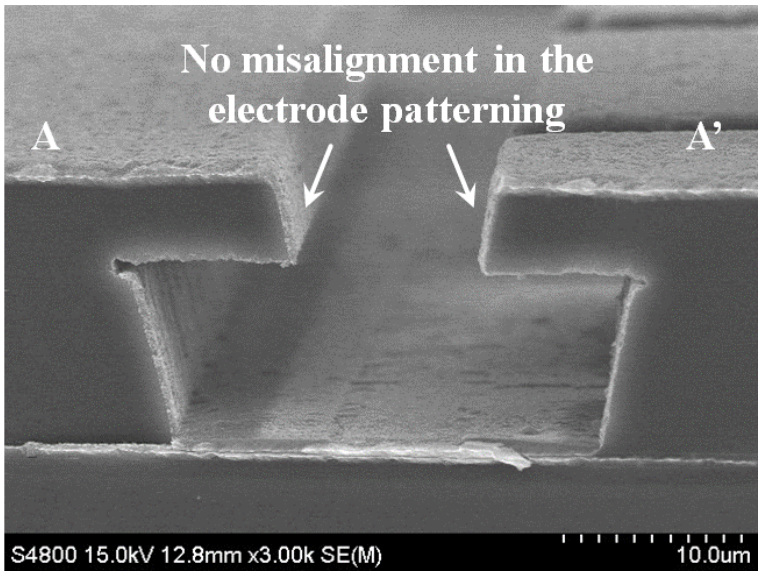
(b) RF electrode and inner DC rail



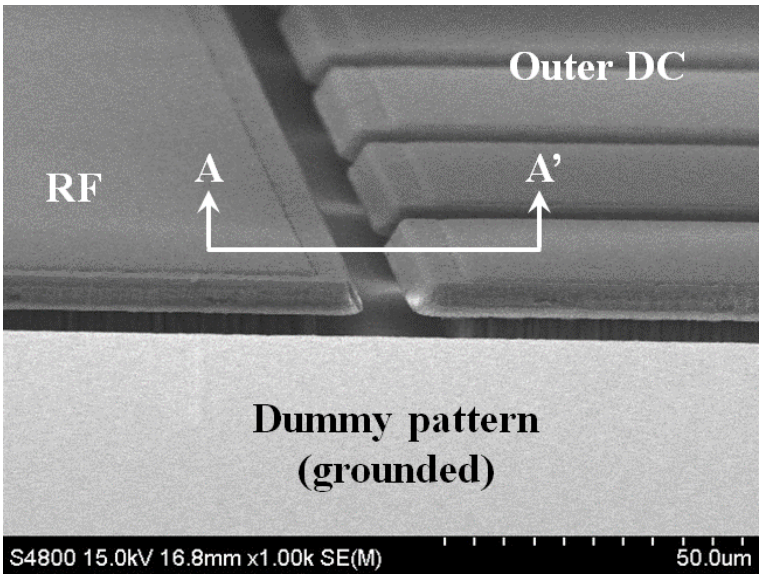
(c) The distance between the electrodes



(d) Colored version



(e) The RF and DC electrodes facing to each other



(b) Tilted view of the RF and DC electrodes

Figure 3-5. Cross-sectional-view SEM images of the trap chip with Al electrodes.

3.3 Gold Coating on the Aluminum Trap

3.3.1 Fabrication Process

Typically, gold is preferred than aluminum as the electrode material of surface ion trap, since the previous researches reported that the native aluminum oxide can contribute to generate additional stray fields [59]. However, the conventional semiconductor processes are scarcely compatible with the gold film on the wafer. Thus, an additional gold coating on the aluminum electrodes after finishing the entire processes is selected for an alternative which is commonly used in the ion-trap community.

The inner DC rails of the proposed chip are laid on the M1 layer, and isolated from the surrounding ground plane with the pattern gaps of 8 μm. Thus, the direct gold deposition on the chip surface can cause the electrical short between the inner DC rail and the ground plane. In order to prevent the case, a shadow mask is used. The shadow mask is made of stainless still and fabricated by a conventional machining process. The layout of the shadow mask and the fabricated shadow mask are shown in Figures 3-6 and 3-7, respectively. Since the gold coating using the shadow mask is proceeded with a die-level process, some manipulative techniques are required. The shadow mask is bonded on a 5-inch photomask with carbon tapes

to be loaded to the manual aligner. The ion-trap chip is aligned with the shadow mask and bonded on the back side of the shadow mask by using the manual aligner. The AZ4620 PR is used for bonding (Fig. 3-8). Then, the shadow mask is loaded on the loading frame which is used for sputtering process by using the interposer pieces. A 10-nm thick titanium layer used as an adhesive layer, and a 100-nm thick gold layer is sputtered on the surface of the shadow mask. After the deposition of gold layer, the chip is separated from the shadow mask by using the photoresist remover solvent.

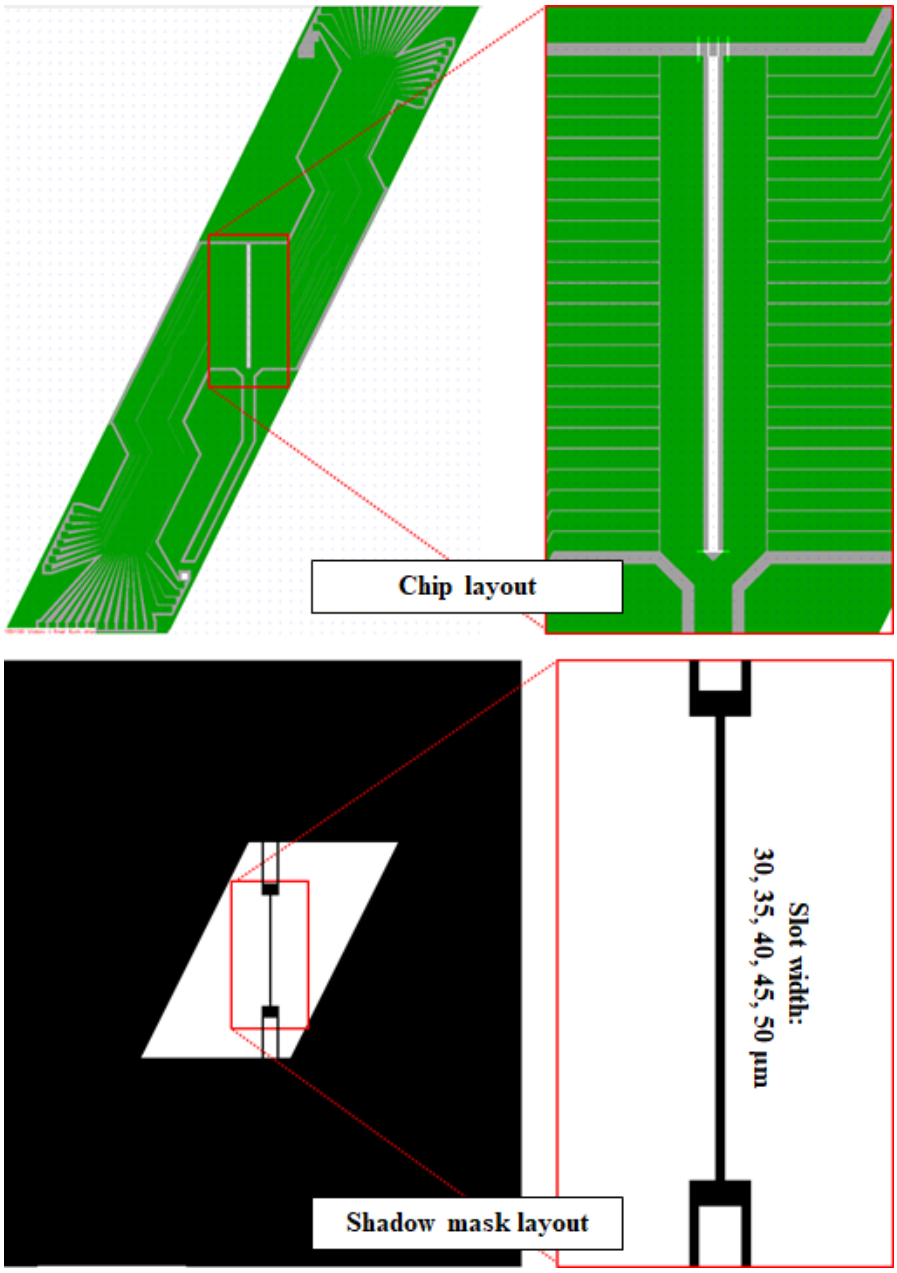


Figure 3-6. Design of the shadow mask.

Figure 3-7. Fabricated shadow mask.

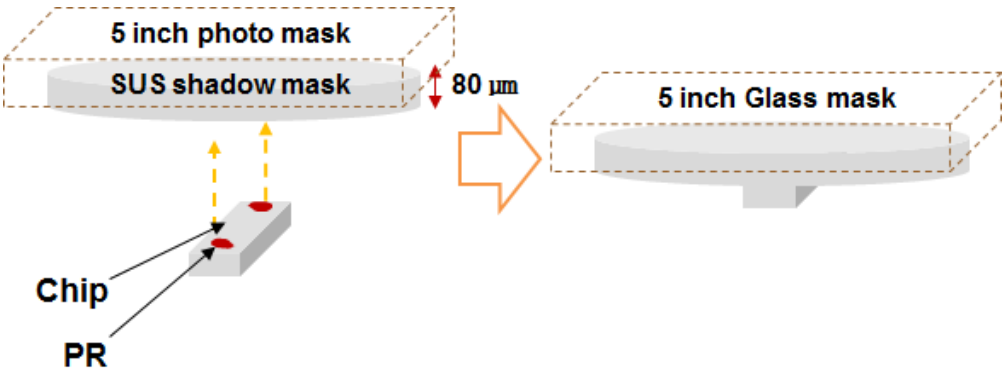


Figure 3-8. Schematic for bonding the chip on the shadow mask.

3.3.2 Fabrication Result

Figure 3-9 is a mosaic optical image of the gold-coated chip. Figure 3-10 shows the top-view SEM images of the chip. The boundary of the shadow mask can be easily distinguished by the images. Figure 3-11 shows cross-sectional SEM images, which show the thickness of the Au layer deposited on the Al electrodes. The thicknesses of the Au layer on the inner DC rail and the top electrode are almost same and approximately 110 nm.

The electrical connections of the electrodes on the chip are investigated again after the gold coating process. After sputtering gold layer on the chip without using the shadow mask, the inner DC rails and the ground plane are shorted. When using the shadow mask, however, all the electrodes including the inner DC rails and the ground plane are electrically opened. Thus, it can be concluded that using the shadow mask for the gold coating process is an effective method.

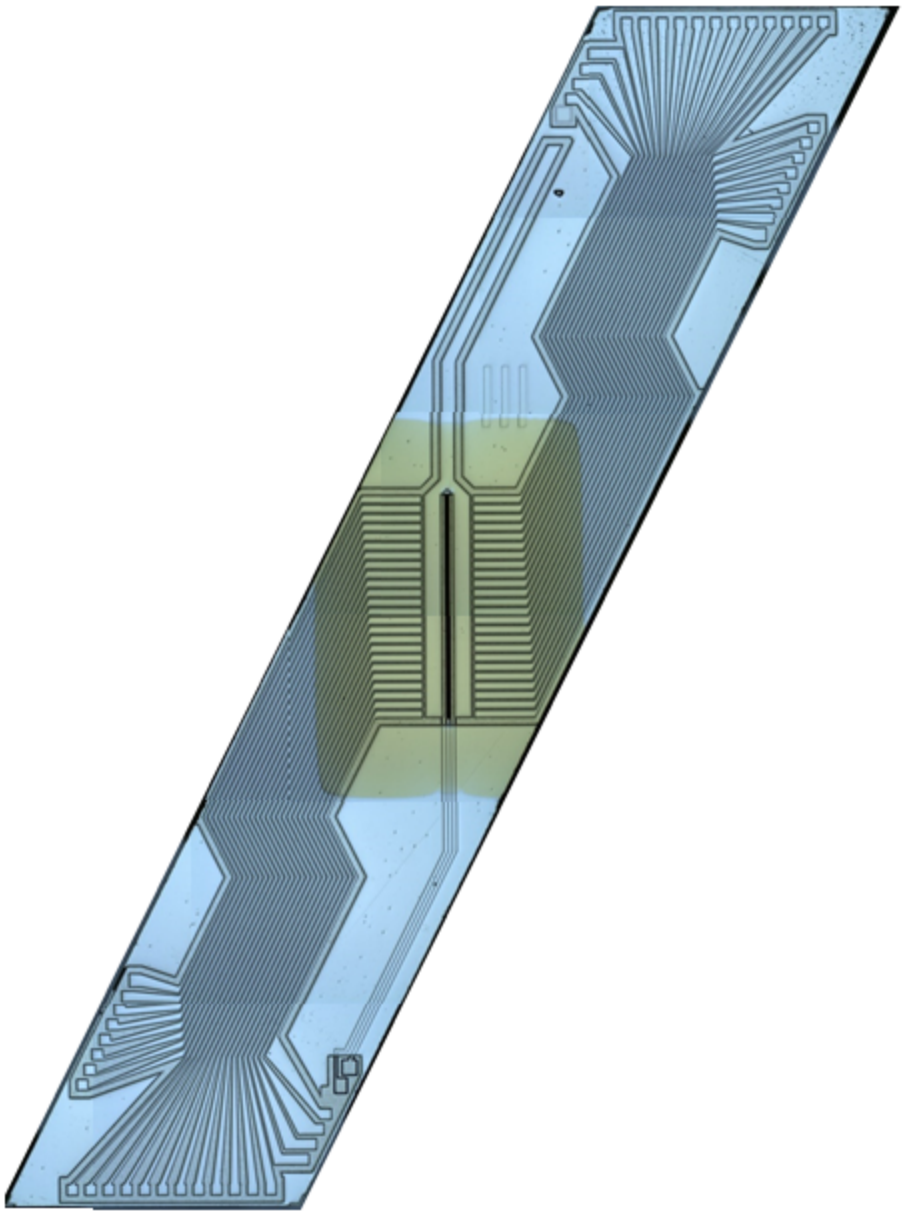
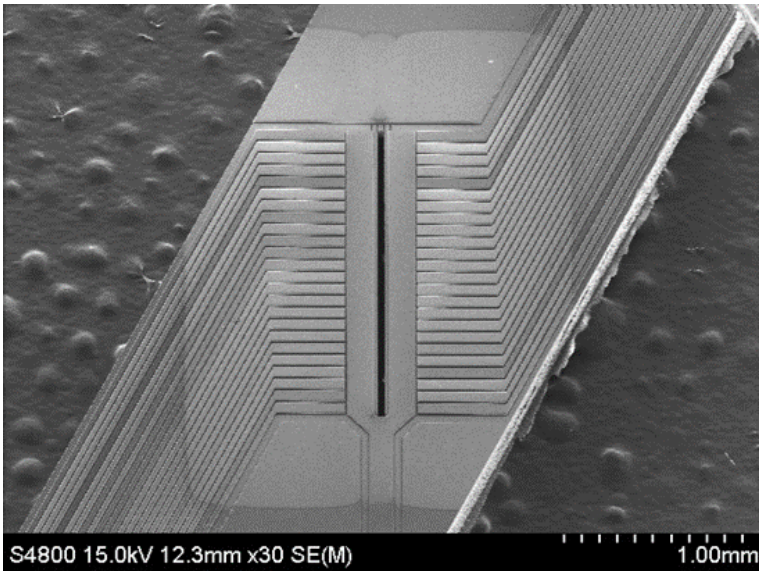
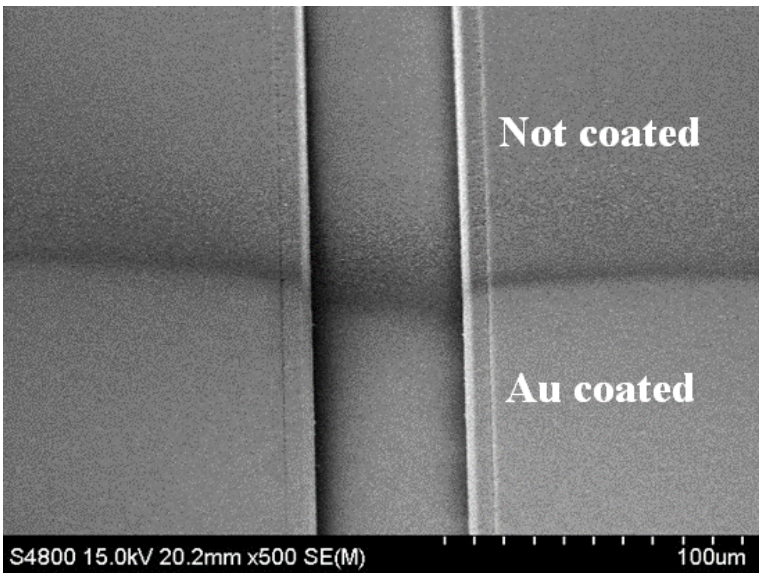


Figure 3-9. Mosaic optical image of the ion-trap chip with gold-coated electrodes.

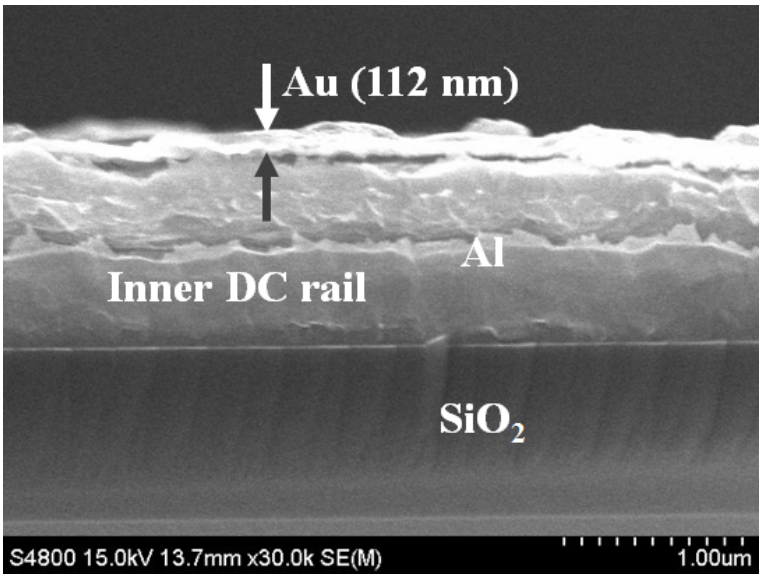


(a) Overview of the chip

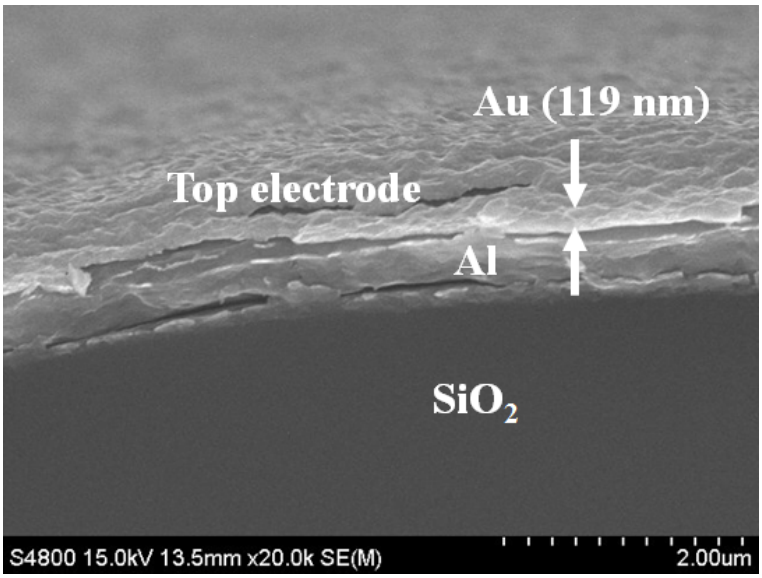


(b) Magnified view showing the boundary of the gold-coated region

Figure 3-10. Top-view SEM images of the gold-coated trap chip.



(a) Au film on the inner DC rail



(b) Au film on the top electrode

Figure 3-11. Cross-sectional-view SEM images of the gold-coated trap chip.

3.4 Chip Packaging

There are a few different alternatives to install the chip inside an UHV chamber [71-73]. Among them, this dissertation uses an approach where the chip is glued on a separate chip carrier. This chip carrier is inserted into a zero-insertion-force (ZIF) socket on a PCB [73]. In the method using a chip carrier and a ZIF socket, the chip is mounted on a chip carrier and electrically connected to the chip carrier by gold bonding wires. The chip carrier should be compatible with a baking process and UHV environment, and the ceramic chip carriers with gold electrodes mentioned in 2.2.3 is are widely used. Especially in the case that the system is designed to load neutral atoms from the backside of the trap chip, a loading hole is fabricated at the center of the chip carrier. In this dissertation, a 3-mm-diameter hole was fabricated by using a conventional drilling press (Fig. 3-12). The chip carrier used in this dissertation has a cavity to hold the chip such that the surface of the chip is recessed compared to the chip carrier body. Therefore, interposer chips should be inserted under the trap chip to allow the laser beams to access the trapping position right above the chip (Fig. 3-13). The interposer chip can be easily fabricated by cutting a bare silicon wafer with a thickness of 650 μm into pieces. To determine the thickness of the spacer chip, the increased height of the overall chip due to the interposer chip and the bonding wires should be taken into account during the chamber design stage. Two silicon spacers can be glued on the chip carrier using a

UHV-rated epoxy compound (353ND, Epotek), with aligning the loading hole fabricated at the center of the chip carrier between the spacers. Then, the ion-trap chip is glued on top of the silicon spacers using the same UHV-rated epoxy.

During the experiments, the RF signal can be coupled to the neighboring DC electrodes, and the RF pick-up will be a source of the stray fields. To filter the RF pick-up instantly, a large capacitor can be mounted on the chip carrier and connected in parallel to each DC electrode. Thus, commercial chip capacitors with the capacitance of 560 pF (116UL561M100TT, ATC) are bonded with a UHV-rated conducting epoxy compound (H21D, Epotek), and connected to the DC electrodes with gold wires. The fabrication result of the chip package is shown in Figure 3-14. The configuration of the chip package mounting the gold-coated chip is different from the aluminum-electrode trap-chip package, since the new version of vacuum chamber is used for testing the gold-coated chip. The internal structure of new vacuum chamber is modified, and the chip need be mounted on the chip carrier with being tilted by 22.5 degrees. The bonding diagram of this case is presented in Figure 3-15, and that of the aluminum trap is already presented in Figure 2-11.

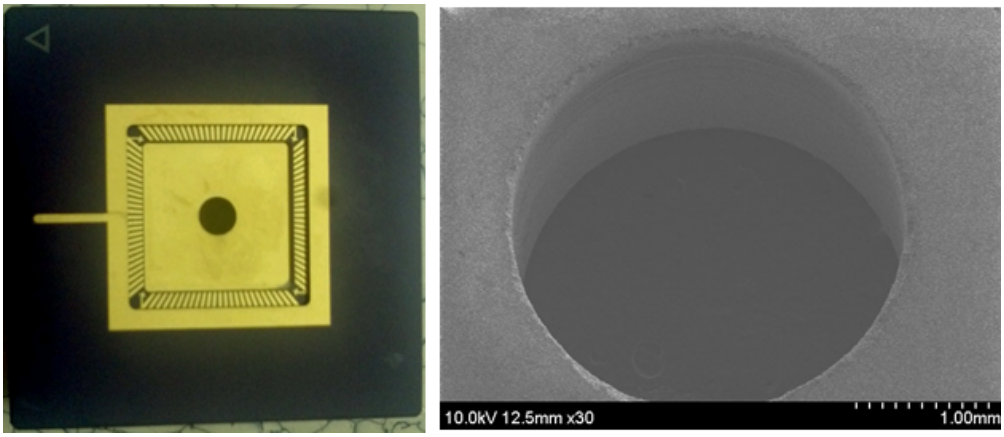


Figure 3-12. Chip carrier with 3-mm-diameter hole and a SEM image of the hole.

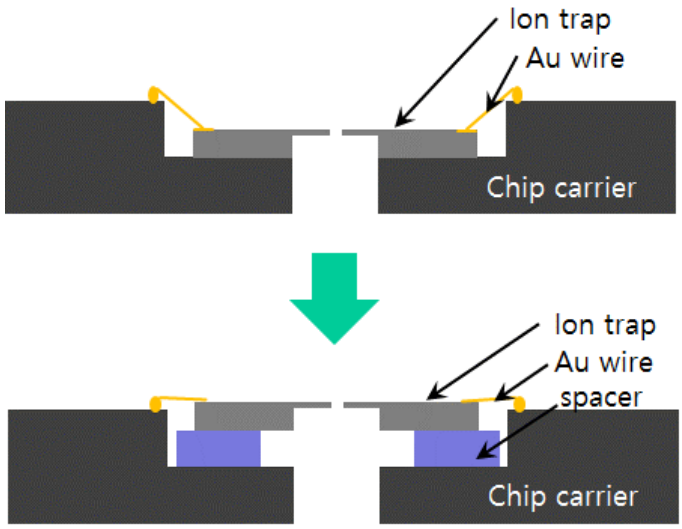


Figure 3-13. Schematic of the necessity of the interposer chip.

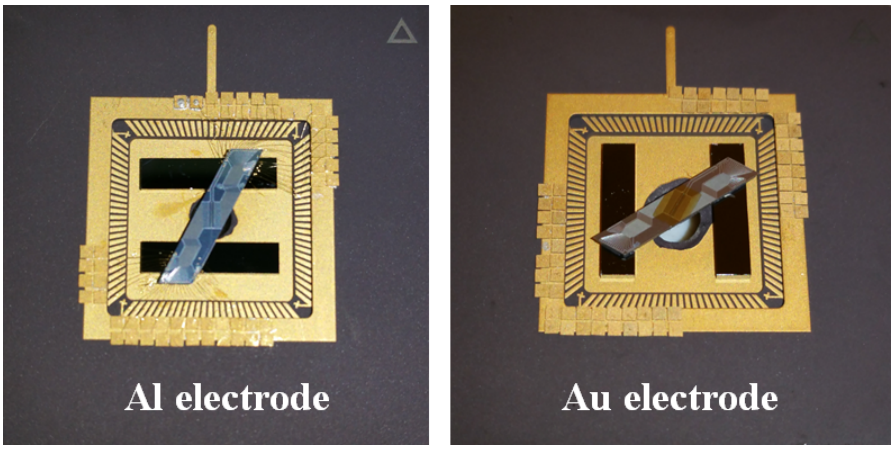


Figure 3-14. Fabrication result of the chip packages.

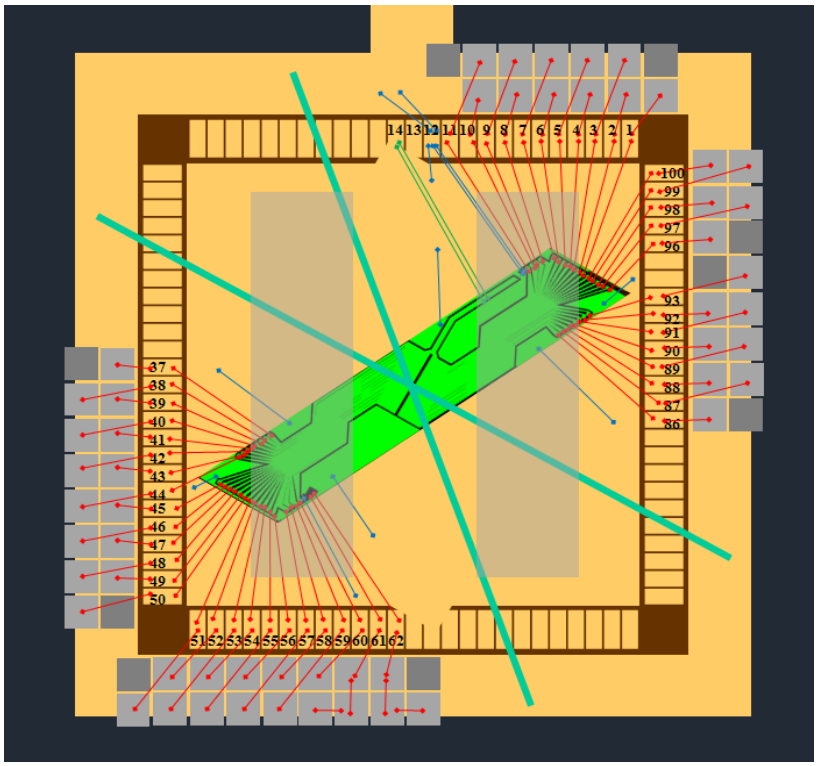


Figure 3-15. Modified version of the wire bonding diagram.

Chapter 4

EXPERIMENTS

4.1 Trapping Ions

4.1.1 Vacuum Chamber and In-Vacuum Components

a. Design and construction of ultra-high vacuum chamber

An overall design of a UHV chamber is shown in Figure 4-1. The ion pump can lower the pressure down to 10^{-10} Torr range, but to reach a pressure below $3x10^{-11}$ Torr, a non-evaporable getter (NEG) pump is added. The trap chip package is installed in a spherical octagon and all experiments are performed around this spherical octagon. In addition to maintaining a UHV pressure, the in-vacuum

components in the spherical octagon should be designed to accommodate as many laser beam paths as possible and also to allow an imaging lens to be placed as close as possible to the chip surface in order to achieve high resolution imaging of the trapped ions with a diffraction-limited, high numerical aperture (NA) lens. Figure 4-2 illustrates the internal structure of the spherical octagon which allows easy installation and removal of the trap chip package. An oven for neutral ytterbium (Yb) atoms and the oven holder should be designed to minimize heat conduction without compromising mechanical stability. Since the tantalum filament can also be evaporated in a high temperature and the evaporated tantalum can short the traces on the PCB, a protective screen is placed between the PCB and the oven supporting layer.

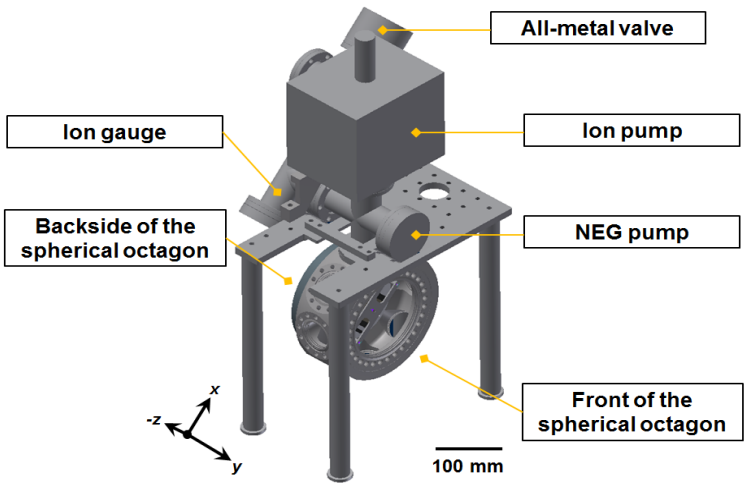


Figure 4-1. Overall design of a UHV chamber.

To find the minimum current which leads to evaporation of the Yb ovens, a residual gas analyzer (RGA) is used to detect the evaporation of Yb atoms. The RGA is temporarily attached to the front 6” conflat (CF) flange of the spherical octagon, and the measurement result with RGA agrees with the expected distribution of the Yb isotopes. For easy installation and removal of the chip carrier, a ZIF socket is mounted on the PCB board as shown in Figure 4-2. All electrical connections on the PCB board are made using press-fit type pins and press-fit type pin sockets to avoid the use of solder in the UHV environment. Figure 4-2 also shows a grounded metal shield between the trap chip package and the recessed viewport to minimize potential disturbance from any stray charges trapped on the front viewport. Before and after the chamber baking, two-types of electrical tests are performed to make sure that there is no electrical problem. To check for any accidental short circuit among electrodes of the ion trap chip, the resistance among the corresponding pins of feedthroughs are measured. To verify the continuity of the electrical connections between all the electrodes and the corresponding pins of feedthroughs, capacitance between each pin and the ground is also measured.

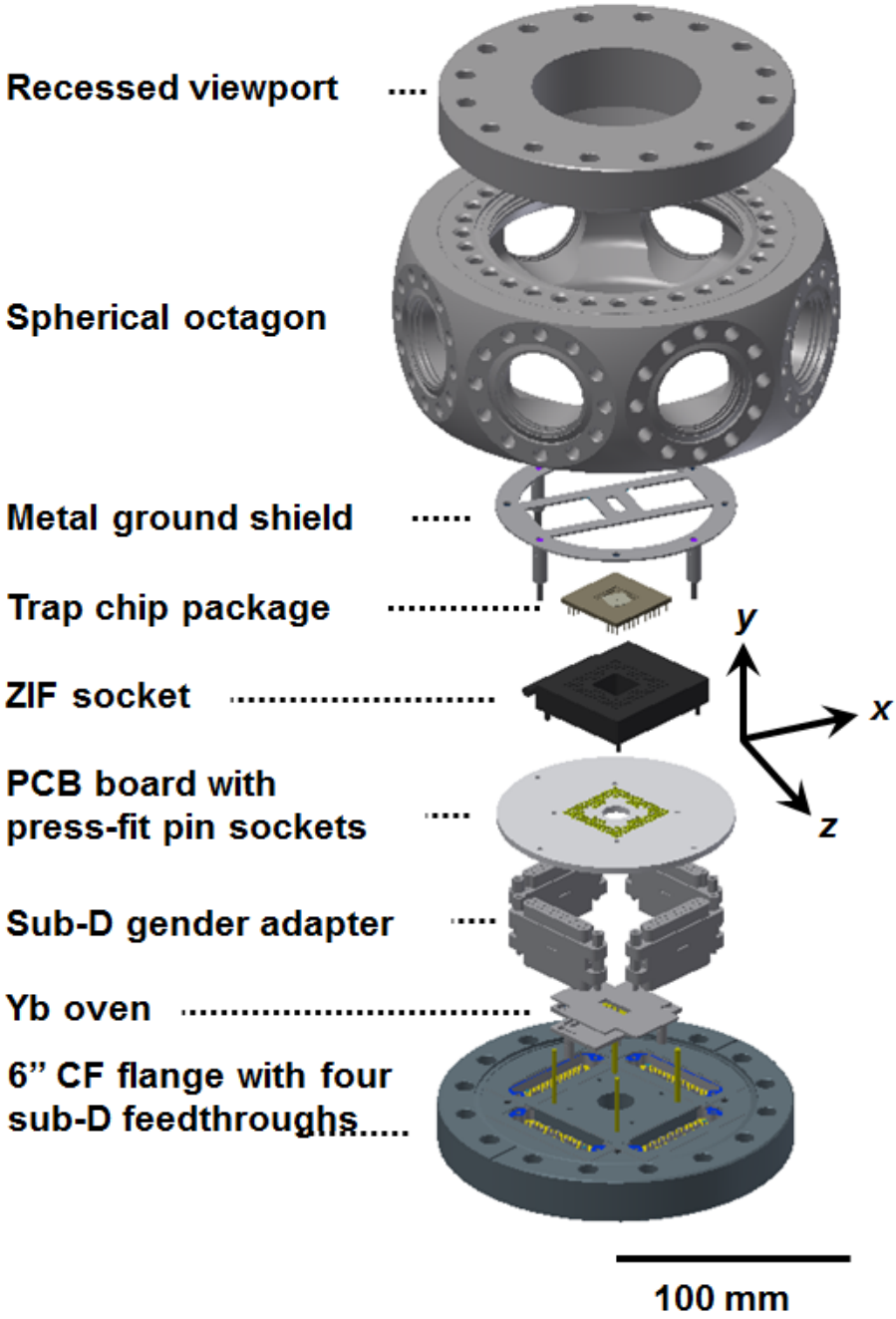


Figure 4-2. Internal structure of the spherical octagon.

b. Details of baking process

To reach a UHV pressure, the entire chamber needs to be baked. Before being baked, the chamber was pumped down with a turbo pump until the pressure reached 10^{-6} Torr range, which generally takes one day. After that, the temperature of the chamber was increased to 200°C at a rate of 0.2°C/min. As the temperature goes up, the pressure starts to increase, but the pressure generally starts to drop in the middle of the ramping process. An ion pump was turned on after the pressure reached the bottom saturation point, and the baking was continued for a few more days. The temperature was ramped down at a rate of 0.2°C/min, and when the temperature reached room temperature, the NEG pump was activated. During the activation process, generally severe outgassing was observed, and the ion pump and ion gauge were switched off when the pressure went above 10^{-5} Torr. Even after the activation, the effects of getter outgassing remained for a long time, and additional baking for a few days was helpful to reach the desired UHV pressure quickly. During this second baking, disconnecting the chamber from the turbo pump can also be helpful to reach a lower pressure. Our ion gauge was housed inside a 2.75" CF tee, and the temperature of the tee surrounding the ion gauge was higher than the rest of the chamber because of the heat generated by the ion gauge filament. To minimize any bias coming from local heating during the pressure measurement, the tee

surrounding the ion gauge was cooled after measuring the final chamber pressure.

4.1.2 Electrical and Optical Setup

a. Electronics

The static voltages applied to the DC electrodes are generated by a multi-channel digital-to-analog converter (DAC) (PCIe-6216V-GL, AdLink). The DAC is connected to the feedthrough at the backside of the UHV chamber. Each channel is connected with an RC filter whose cut-off frequency is approximately 300 kHz to filter the RF pick-up at the outside of the chamber (Fig. 4-3).

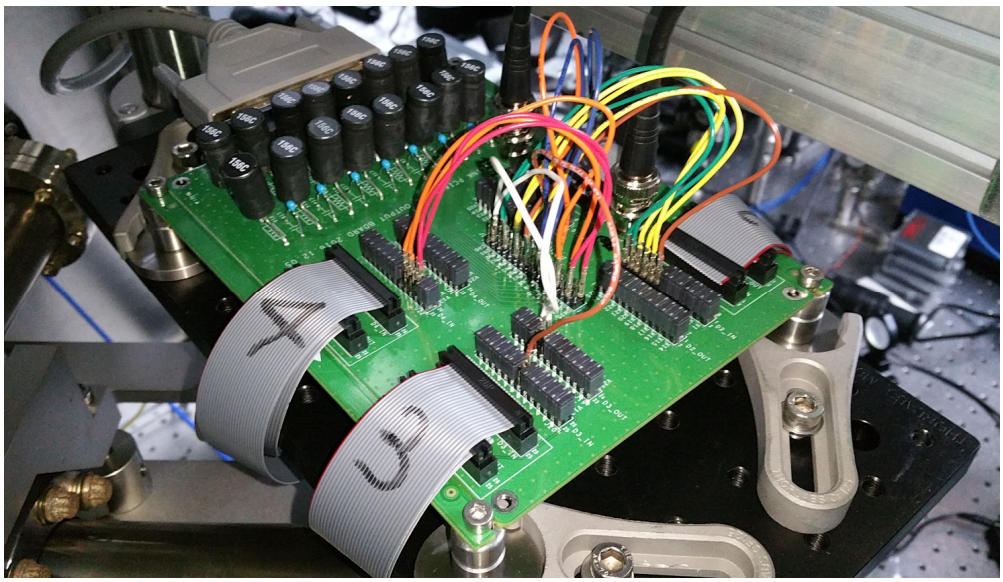


Figure 4-3. RC filter board at the outside of the chamber.

The RF signal for the radial confinement of the ions is generated by a signal generator (SG384, Stanford Research Systems, Inc.) The signal is amplified by a helical resonator [74, 75]. It is mainly composed of two copper cylinders, and each has a copper coil in it. The cylinders are assigned coaxially, and fixed by an additional copper cap (Figs. 4-4). The resonance frequency of the helical resonator is designed to be equal to the RF trap frequency, 31.84 MHz in this case. After assembly of the helical resonator, the position of the cap must be coarsely tuned to find the resonance frequency. The back reflection of the RF signal is monitored by using a directional coupler and a spectrum analyzer (Fig. 4-5), and the lock the position of the resonator cap after finding the global minimum of the reflected power. The quality factor Q can be measured by the same setting. The quality factor is determined by the ratio between the resonance frequency and the bandwidth of full width at half maximum of the monitored curve, and approximately 100 for our case.

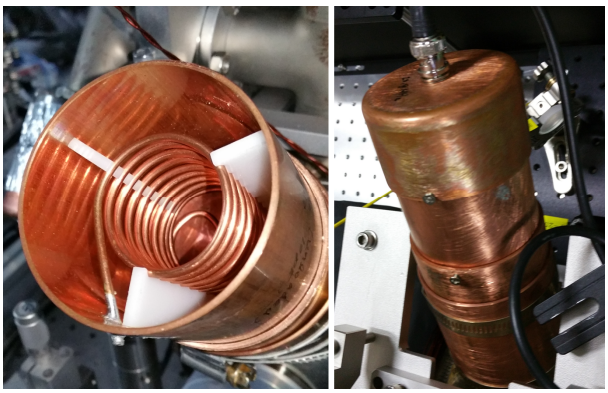


Figure 4-4. Helical resonator before and after fixing the cap.

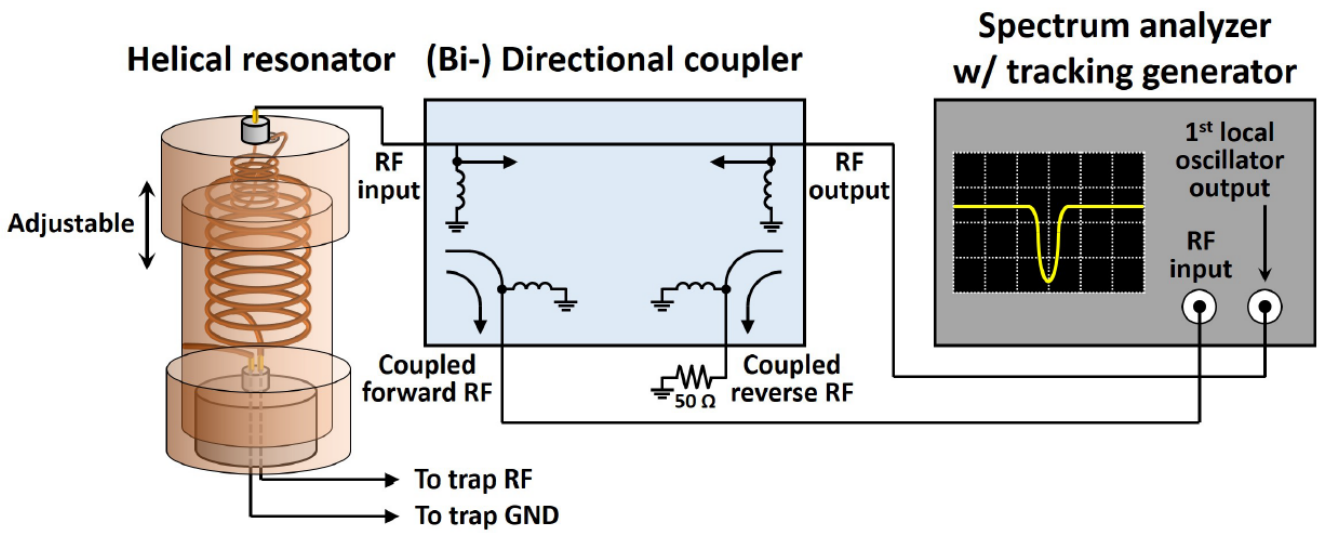


Figure 4-5. Electrical connections of a directional coupler and a spectrum analyzer.

b. Lasers

In our setup for trapping $^{174}Yb^{+}$ ions, the main function of the 369.5-nm laser is Doppler cooling of the Yb ions. A typical ion trap experiment uses a single beam path, so to cool the motion of the ions along all three principal axes of the total potential, the beam path is chosen to be not orthogonal to any of three principal axes. If symmetric voltages are applied to the DC electrodes, one of the principal axes will be parallel to the y-axis, but this is orthogonal to the momentum vector of the laser so the cooling efficiency along this axis will be compromised. To avoid this problem, two principal axes in the radial direction (xy-plane) are tilted with respect to the geometry of the chip by applying asymmetric voltages. In our setup, the surface trap chip is mounted at a 45° angle with respect to the optical table so that the beam path of the cooling laser can be set parallel to the optical table.

The 935-nm and 399-nm lasers are set to co-propagate from the opposite side of the chamber as shown in Figure 4-6, but there are also many other ways to set the laser paths. The first factor to consider is the orientation of the magnetic field and the polarization of the laser that depend on the selection rule. Other factors to consider include the imaging scheme, scattering from the bonding wires, spatial constraints coming from the chamber dimension, availability of proper optical components, convenience of the optical setup, and plans for future experiments. For

example, one way to make all three lasers meet at the trapping position is to combine all the beams parallel to each other with some space, and focus them together using a single achromatic lens. However, in our setup, co-propagating setup was chosen because of the unavailability of an achromatic lens with proper anti-reflection (AR) coating and the focal length suitable for our vacuum chamber design and chip dimension.

The frequencies of lasers are locked by a proportional–integral–derivative (PID) controller. The controller is a homemade software based on MATLAB and uses the frequency measured by a wavelength meter (WSU-2, High Finesse). The details of laser stabilization are not discussed in this dissertation.

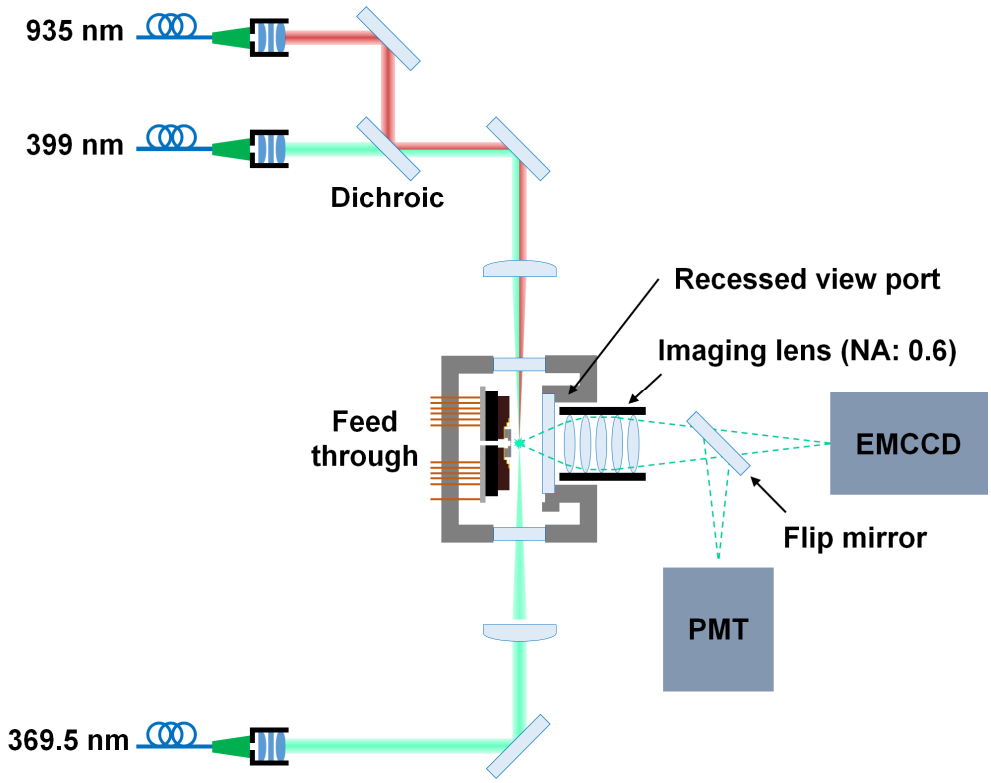


Figure 4-6. Schematic of optical setup for trapping $^{174}Yb^{+}$ ions.

c. Imaging

To maximize the collection efficiency of the emitted photons from the trapped ion, an imaging lens with high NA and a custom-made recessed viewport are used as shown in Figure 4-6. The imaging lens has NA of 0.6 and AR coating for 369.5 nm and it is designed to be diffraction-limited at 369.5 nm. The expected magnification of the lens was 8.6 from the numerical simulation, and it was confirmed by the

actual measurement of 8.9(1) which was obtained by comparing the image size of electrodes monitored by an electron-multiplied charged-coupled-device (EMCCD) (DU-897U-CS0-EXF, Andor Technology) and the mask design of the ion trap chip. The difference is expected to be caused by the non-optimal alignment of the imaging system. The working distance is 17.2 mm including 4-mm thick viewport, and if different thickness of viewport is chosen, the simulation shows that it becomes difficult to achieve diffraction-limited resolution. Figure 4-2 shows that our system is composed of multiple components, and the height of each component has some amount of uncertainty. The depth of the recessed viewport is determined considering the amount of inaccuracies in fabrication and assembly.

4.1.3 Trapping Ions

After the preparations of the vacuum chamber, electronics, and optical setup, trapping ions is relatively straightforward. The RF generator is set to supply 0.8~1.5 $V_{p\text{-}p}$ at the corresponding frequency for the helical resonator, and the signal is amplified by the helical resonator. A DC voltage set is applied to the chip by the connected DAC. Figure 4-7 shows an example DC voltage set which has been used in our setup, but these values are slightly changed every day to find optimal position of the DC null. The trapped ions can be observed by both an EMCCD and a monochrome CCD (1501M-USB, Thorlabs). The 369.5-nm, 399-nm, and 935-nm

lasers are injected to the point where the ions will be trapped. The Yb oven is heated to evaporate the neutral Yb atoms. The current of 2.6 A and the voltage of 4.15 V are supplied to the oven. A few minute after the oven is turned on, the trapped ions can be observed by the CCD camera. If the oven is not turned off after the ion is trapped, the number of trapped ions increases up to 20 (Fig. 4-8). This number is determined by the axial DC potential

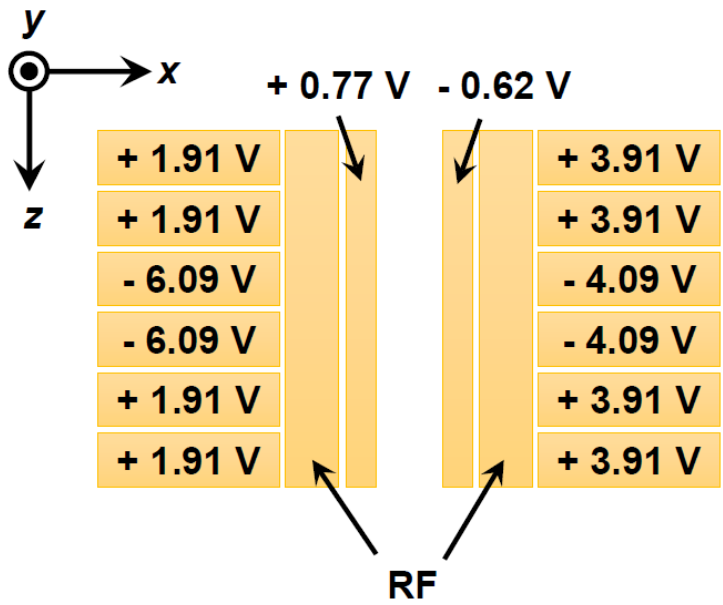


Figure 4-7. An example of the DC voltage set used to trap ions.

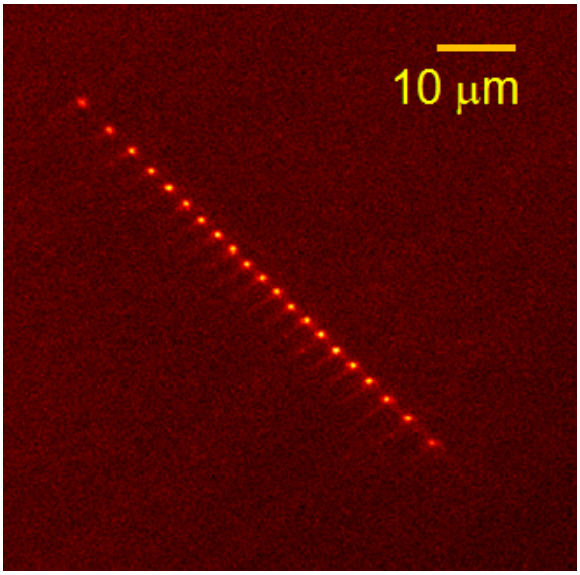


Figure 4-8. EMCCD image of twenty $^{174}Yb^{+}$ ions trapped on the fabricated chip.

4.2 Dielectric Charging

4.2.1 Experimental Setup

The electrode structure proposed in this dissertation aims to suppress the generation of stray fields from the static charges accumulated on the dielectric surfaces. To investigate the effectiveness of the proposed structure, UV laser is injected perpendicularly to the chip surface to intentionally generate the static charges. A mode-locked pulse laser with a wavelength of 355 nm (Paladin, Coherent) is used for the UV laser, and the corresponding delivered energy of the

wavelength is 3.4 eV. The optical setup for injecting 355-nm laser is shown in Figures 4-9, 10. The uncollimated 355-nm laser is guided to the front view port of the vacuum chamber by a selective mirror, and focused to the ion position by the imaging objective. The measured reflectivity of the selective mirror is approximately 4%. One more 355-nm laser should be delivered to the chamber to shine the whole chip surface to identify where the perpendicular beam is spotted. This setup is shown in the upper-right inset of Figure 4-10.

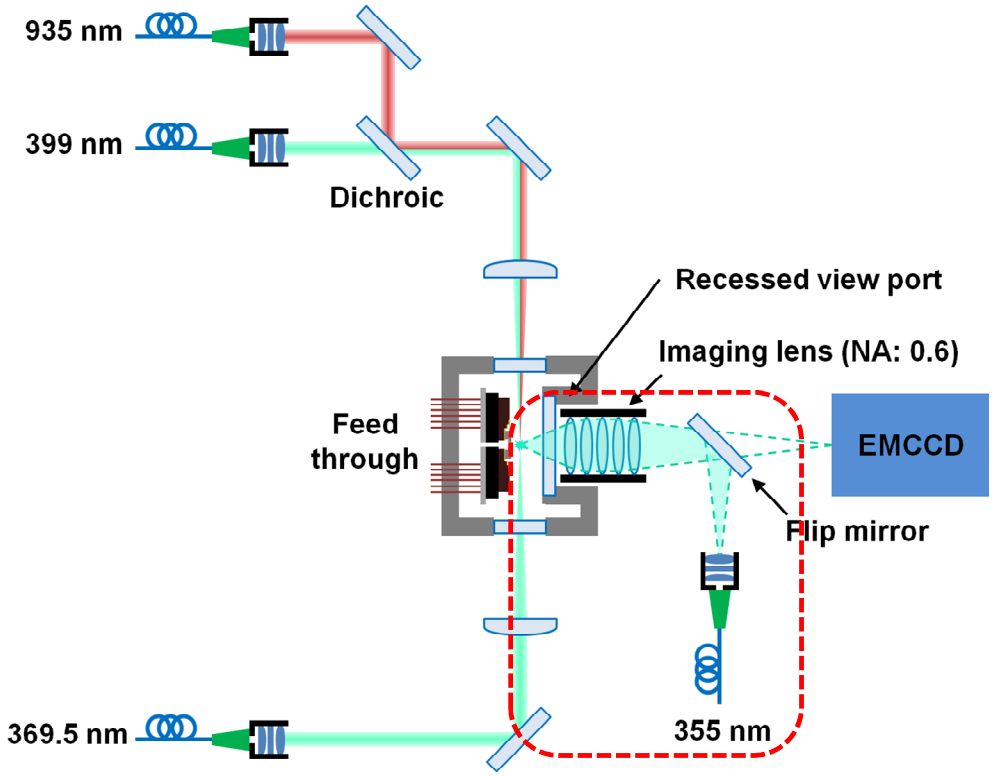


Figure 4-9. Schematic of optical setup for injecting 355-nm laser to the chamber.

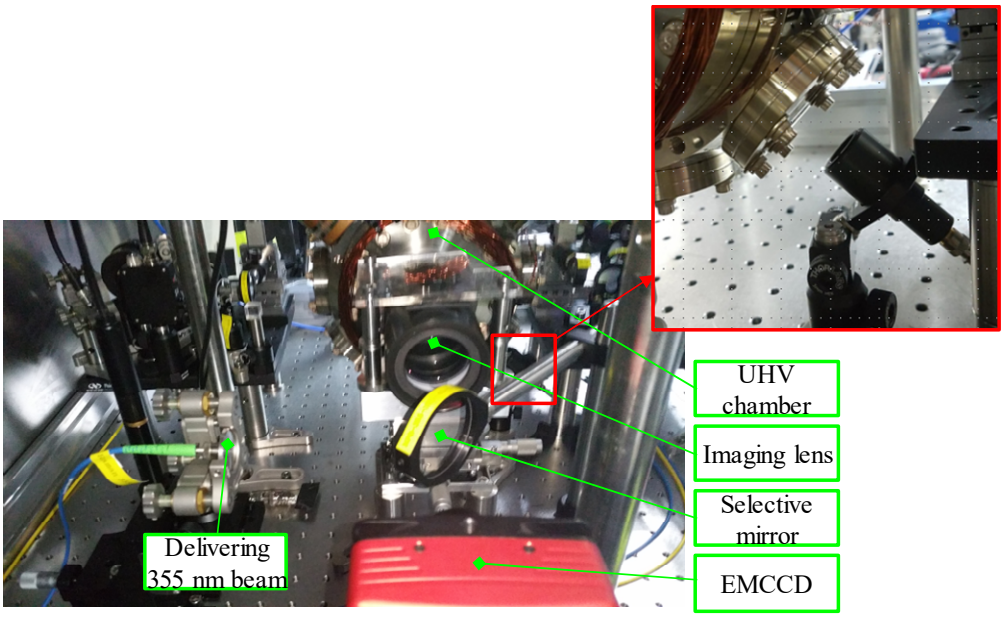


Figure 4-10. Experimental setup for the charging experiments.

The position of the front UV beam is controlled by servo motors (Z812B, Thorlabs) connected to the micro-manipulator and MATLAB software (Figure 4-11). This system automatically moves the beam position, which in turn allows for scanning the charging effects according as the position of the beam spotted, whereas the previous researches about the charging effects injected the UV beam on a specific spot [55, 56] or illuminated global beam to generate static charges [59].

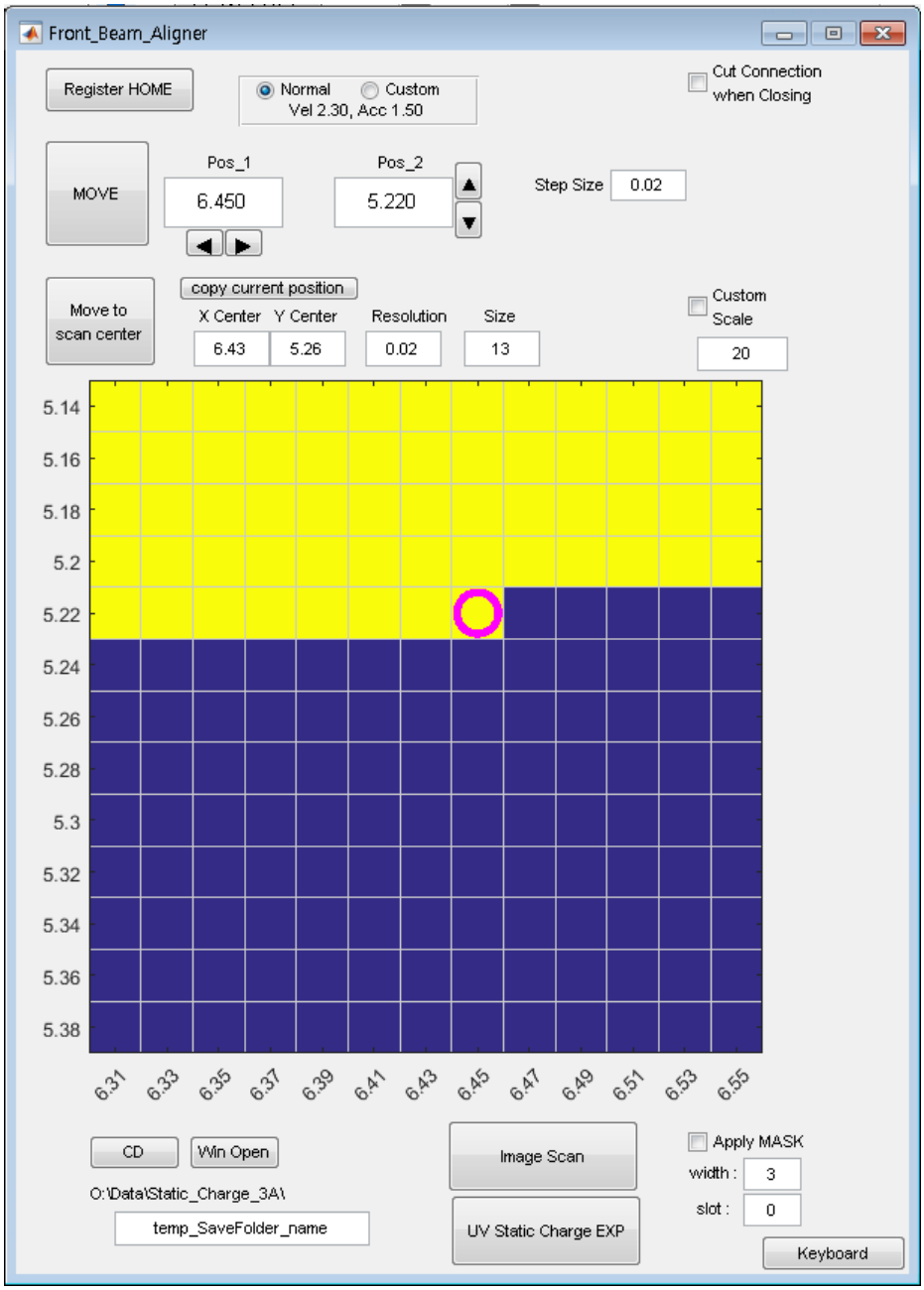


Figure 4-11. Software interface of the front beam aligner.

The displacement of the ion position after injecting the laser is calculated by comparing the EMCCD images captured before and after the laser injection. The peak pixel in the image is obtained by a fast Fourier transform function in MATLAB, and the value of ion shift is provided in the unit of EMCCD pixel. In addition, if the ion position is shifted, the ion should be moved back to the its original position to continuously iterate the same experiments, because the accumulated charges are expected not to easily dissipate. Therefore, the axial potential is briefly moved toward the opposite direction of the potential shift induced by the stray field, to compensate the shift of ion position (Figure 4-12). These steps are also implemented by MATLAB software, and the interface is shown in Figure 4-13.

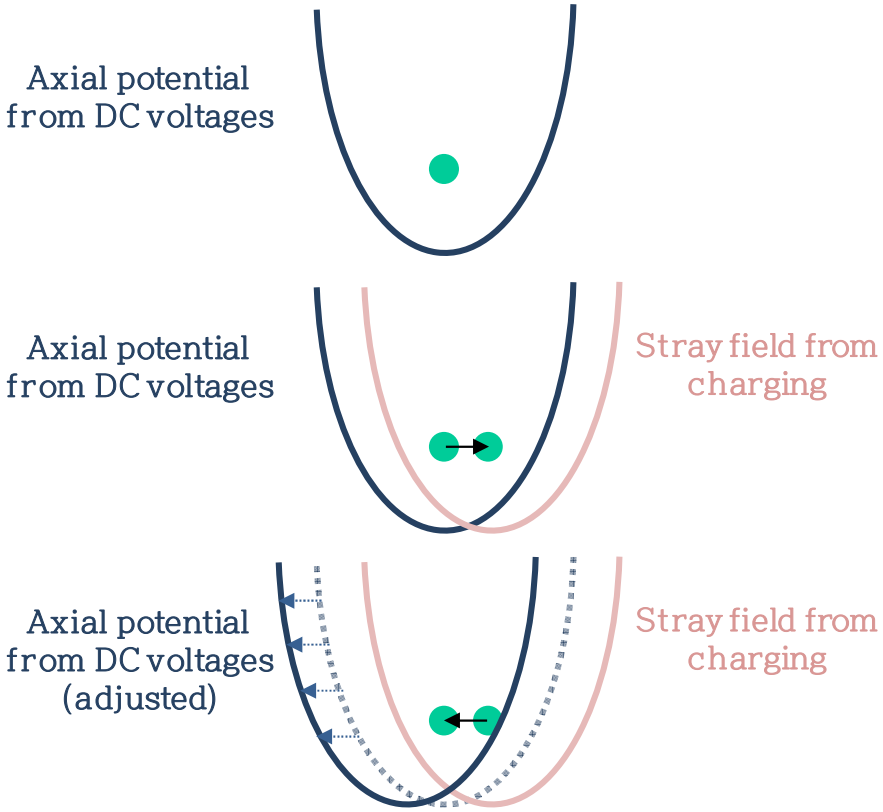


Figure 4-12. Schematic of the compensation procedure of the shifted axial potential.

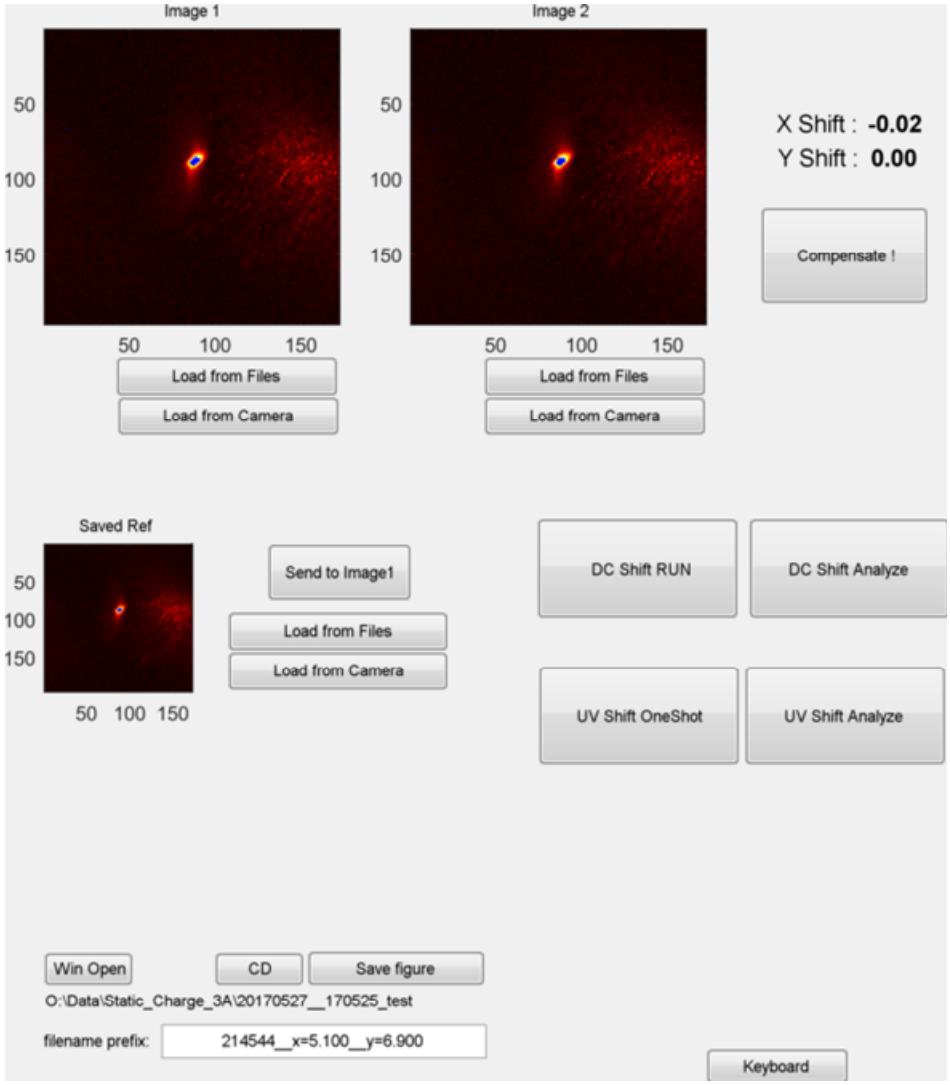


Figure 4-13. Software interface of the ion shift analyzer.

The raw data from the ion shift analyzer is provided in the unit of pixels in the EMCCD image. Therefore, effects of the axial electric potentials which impede the ion displacement cannot be reflected to the experimental results. In order to

transform these data to the stray fields, the measured values of ion displacement and the simulated values of stray fields when a specific DC voltages set is applied to the DC electrodes are used. When applying DC voltages presented in Figure 4-14 in addition to the DC voltages for trapping ions axially, the ion shifts in the EMCCD pixel unit are measured for the three different trap chips, and the results are 10, 3, and 14 pixels, respectively. Also, the stray fields at the ion position generated by the DC voltages in Figure 4-14 are obtained by BEM simulations, and the results are 5.13, 1.93, and 1.93 V/cm, respectively. By using these values, the data in EMCCD pixel unit can be converted to the stray fields. After this procedure, the effects of charging can be represented with the absolute value of stray fields, then the effects can be compared among the different experimental sets.

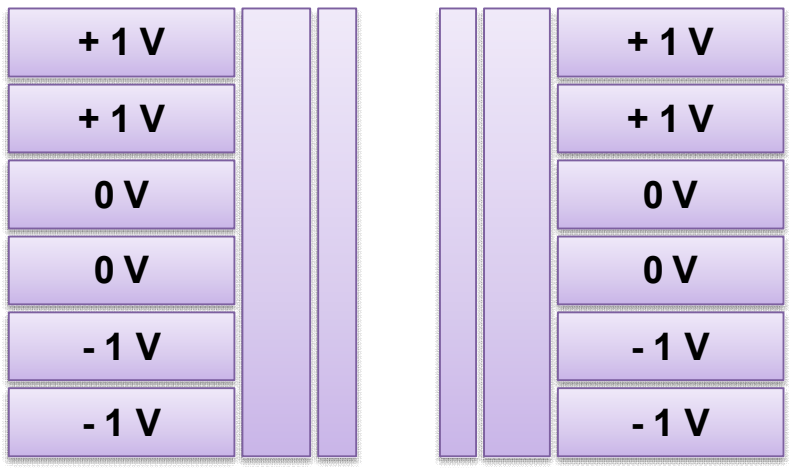


Figure 4-14. DC voltage set used in the conversion of raw data to stray field.

4.2.2 Experimental Result

In this dissertation, the charging effects are investigated for the three different types of ion trap chips which have the exposed sidewalls of the dielectric pillars, the Al-coated dielectric pillars, and the Au-coated dielectric pillars. The exposed time, the estimated beam power at the chip surface, and the spot size of the 355-nm laser are 0.5 second, 40 μW, and approximately 8 μm, respectively. Figures 4-15~17 shows the experimental results. The size of each pixel is 16 μm, and the color at each pixel represents the displacement of ion position when the perpendicular beam is spotted at the pixel position. The yellow and blue colors represent stray field to the lower-right and the upper-left direction, respectively. The scale bars are equivalent to every experimental sets.

In the charging experiment using the ion trap chip with the exposed dielectric sidewalls, the charging of dielectric sidewalls is clearly shown (Fig. 4-15). In the case that the 355-nm laser is injected near the edge of the electrodes, the intensity of stray fields is obviously higher than the case of laser injecting on the surface of the electrodes. It is shown that the trapped ion with a positive charge is repulsed from the laser-injected point by the positive charges accumulated on the dielectric sidewalls of the pillar structure. However, the attraction of the ion by the negative charges accumulated in the native aluminum oxide is not observed even though the

chip has aluminum electrodes. The maximum and minimum intensity of the stray field in this experimental set are 22.5 and -25.8 V/m, respectively, and the standard deviation of the stray field intensity is 3.53 V/m.

The result of charging experiment using the ion trap chip with the Al-coated dielectric side surfaces is presented in Figure 4-16. Different from the first experimental set, the repulsive charging effect is not clearly observed in this experimental set, because any surface of the bare dielectric pillars is revealed to the

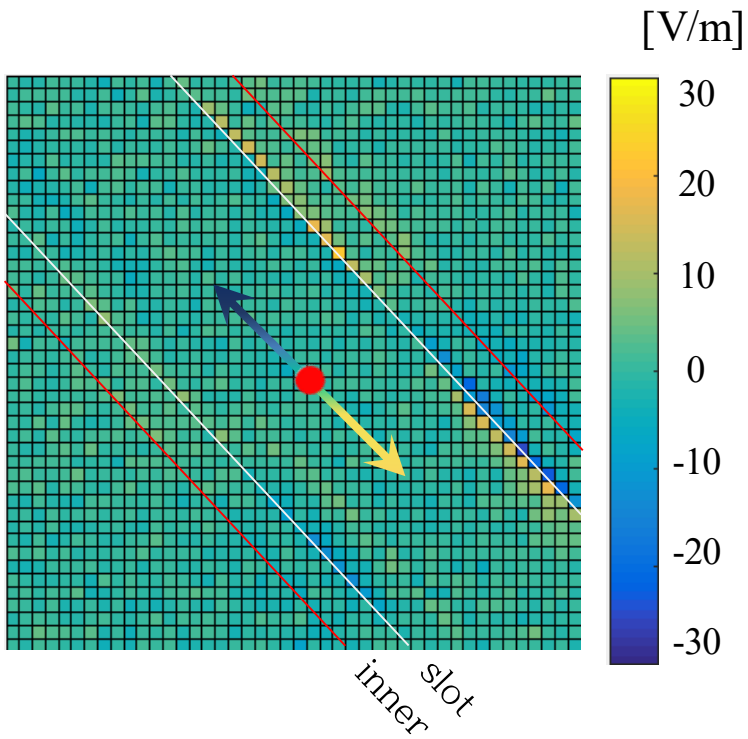


Figure 4-15. Experimental result of the trap chip with exposed dielectric sidewalls.

trapped ion. However, the attractive movement of the trapped ion by the negative charges in the native aluminum oxide layer is clearly shown. Note that the directions of stray fields in Figures 4-15 and 16 are opposite. The maximum and minimum intensity of the stray fields in this experimental set are 22.3 and -25.5 V/m, respectively, which are very similar to the results of the previous experimental set. The standard deviation of the stray field intensity is 5.63 V/m.

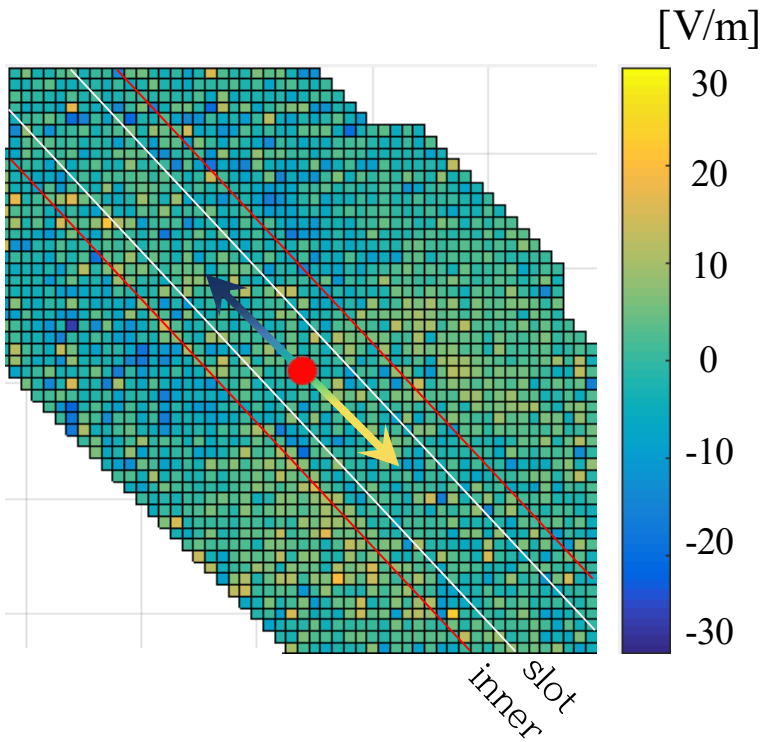


Figure 4-16. Experimental result of the trap chip with Al-coated dielectric sidewalls.

The experimental result using the Au-coated chip is shown in Figure 4-17. In this case, the intensity of the stray field is from -9.75 V/m to 4.78 V/m, which are even lower than the previous cases. Moreover, the relatively high field intensity is measured when the laser is injected near the loading-slot region including the surface of the inner DC rails. This effect seems to arise from the charging of the silicon sidewalls near the loading slot which is revealed to the ion position. The stray field generated by the charging of the top-layer electrode surface or the sidewalls are very low (under 1 V/m) and cannot be clearly distinguished from the ion shift by the ion micromotions from the other sources. In addition, the standard deviation of the stray field intensity is 1.56 V/m, which is even lower than those of the experimental results using the ion-trap chips with Al electrodes.

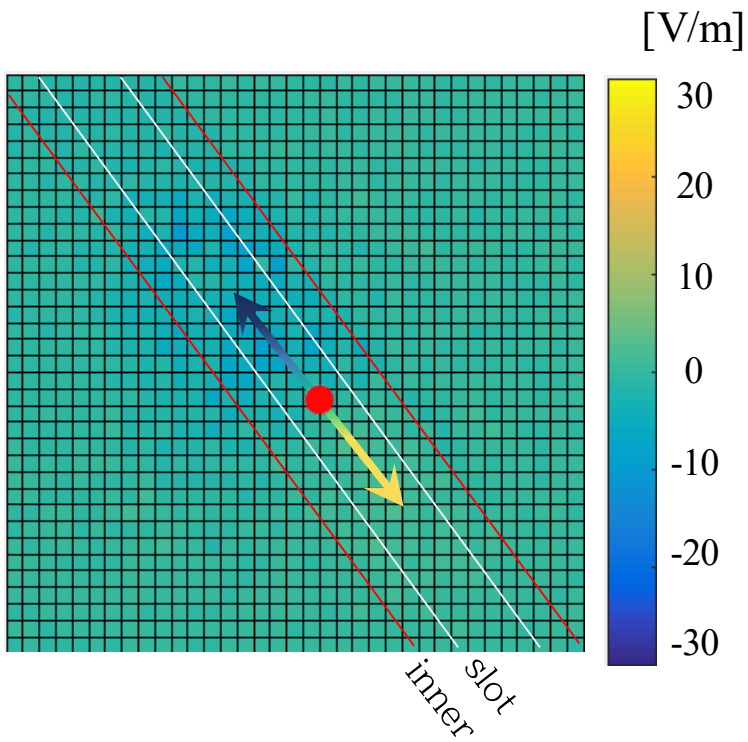


Figure 4-17. Experimental result of the trap chip with Au-coated dielectric sidewalls.

Chapter 5

CONCLUSIONS AND FUTURE WORKS

5.1 Conclusions

This dissertation presented a silicon surface ion-trap chip with dielectric sidewalls shielded by metal films. In the proposed structures, the dielectric pillars supporting the top electrodes had overhang structures. The upper and lower part of the pillars would be coated by separate aluminum layers to protect the dielectric surfaces not to be revealed to the trapped ions.

The design of chip layout was based on BEM simulations. The validity of the BEM simulation tool was verified by comparing the simulation results of the simple

electrode structures with the analytic solutions and the simulation results of the practical complex trap-chip structures with the experimentally measured values. The design procedure of the RF electrodes aimed to achieve a deep trap depth with the q-parameter of 0.25, and the simulated value of the trap depth and the ion height were 0.329 eV and 63 μm, respectively, with assuming the RF voltage amplitude of 300 $V_{p\text{-}p}$ at the RF frequency of 50 MHz. The chip shape was designed to decrease the beam scattering by the chip body considering the beam paths in the horizontal and the anti-diagonal directions.

A sacrificial process was designed to fabricate the overhang structure of the oxide pillars, and polyimide was chosen for the sacrificial material. The ion-trap chip with aluminum-coated dielectric sidewalls of oxide pillars was fabricated by the designed process. Additional die-level process was developed for gold coating on the fabricated chip by using a shadow mask. The fabricated chip was packaged on a commercial chip package and inspected for the electrical connections.

The experimental setup for trapping $^{174}Yb^{+}$ ions was prepared. A vacuum chamber with in-vacuum electronics was constructed. Electrical setup including a helical resonator and a DAC was connected to the inside of the vacuum chamber via electric feedthroughs. Three lasers were delivered to the ion-trap chip, and imaging setup was placed in front of the chamber. The ions can be trapped straightforwardly

with the prepared setup.

The effects of dielectric charging were investigated by injecting a UV laser to the trap chip in the perpendicular direction, to evaluate the effectiveness of the proposed electrode structure. The intensity of the stray field was estimated by measuring the displacement of ion position when charging is induced. In the charging experiment using the ion trap chip with the exposed dielectric sidewalls, the maximum and minimum intensity of the stray field were 22.5 and -25.8 V/m, respectively, and the standard deviation of the stray field intensity was 3.53 V/m. When using the ion- trap chip with the Al-coated dielectric side surfaces, the maximum and minimum intensity of the stray fields were 22.3 and -25.5 V/m, respectively, and the standard deviation of the stray field intensity was 5.63 V/m. The experiments using the Au-coated chip resulted the intensity of the stray field from -9.75 V/m to 4.78 V/m, and the standard deviation of the stray field intensity is 1.56 V/m.

These experimental results indicate that the proposed electrode structures can suppress the stray fields from the dielectric charging effects by preventing the exposure of dielectric side surfaces to the trapped ions. In addition to the electrode structures with overhung dielectric pillars, the gold coating on the aluminum electrodes surfaces is also required to eliminate the stray fields induced from the

native oxide layer grown on the aluminum electrodes. The micromotions from the sources including non-ideal fabrication of trap chips, inaccuracies of the electric field simulations, and contaminants on the electrode surfaces can be compensated by finely tuning the DC voltages, after the ions are trapped. However, the micromotions induced by the built-up charges cannot be eliminated before qubit operations, since they are occurred by photo-electric effects during the experiments using UV lasers. Therefore, the only way to avoid the micromotions induced from the static charges is the realization of the appropriate chip structures which entirely shield dielectric surfaces not to be exposed to the trapped ions. Regarding this aspect, the ion-trap chip presented in this dissertation can provide a significant breakthrough which can be widely applied to various ion-trap applications utilizing surface ion-trap chips.

5.2 Future Works

The charging experiments presented in this dissertation was performed only with the fixed exposure and power of UV laser. Thus, effectiveness of the proposed structure need be investigated for the different conditions.

The stray fields generated by the charges accumulated on the silicon sidewalls exposed near the loading slot is not overcome in this dissertation. The exposure of silicon substrate can be prevented by the fabrication of angled sidewalls of the

substrate near the loading slot. Currently, our group is developing the wet-etching of silicon substrate from the back side of the wafer, before fabricating electrode structures presented in this dissertation on the front side of the wafer. The ion-trap chip with angled silicon sidewalls as well as the electrode structures entirely protected by gold films can be more tolerant to the generation of photoelectric charges and stray fields.

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국문 초록

이온트랩은 전자기장을 이용하여 공간 상에 하전입자를 포획하는 장치이다. 이온트랩에 포획된 이온은 레이저나 마이크로파를 이용하여 그 양자 상태가 제어될 수 있으며, 주변 환경으로부터 영향을 거의 받지 않아 양자 상태의 결맞음 (coherence) 시간이 매우 길다. 이러한 장점으로 인해 이온트랩 기술은 현재 가장 각광받는 양자 플랫폼의 하나로 평가 받는다. 이온트랩은 보다 복잡한 양자 알고리즘의 구현에 필요한 대규모 집적 이온트랩의 구현을 위해, 미세전기기계 시스템 (micro-electromechanical system, MEMS) 칩으로 제작되기 시작하였다. MEMS 이온트랩 칩의 사용은 이온트랩 구조의 확장성 확보와 몇몇 실험부품의 칩 내부 집적 등을 가능하게 하였으나, 몇 가지 문제점도 함께 유발하였다. 대표적인 문제점 중 하나는 전극을 지지하기 위한 두꺼운 절연층 측벽이나, 금속 표면의 자연 산화막에 축적된 전하로 인해 발생하는 표유전계 (stray field) 이다. 표유전계는 이온의 미세움직임 (micromotion) 을 발생시켜, 이온의 가열 및 이탈 등을 유발할 수 있다. 본 학위 논문에서는 절연층 측벽을 금속 박막으로 보호한 실리콘 평면 이온트랩 칩을 제안한다. 전극을 지지하는 절연층 기둥은 돌출 구조를 가지도록 제작되며, 절연층 기둥의 아랫 부분과 아랫 부분으로부터 돌출된 윗 부분은 각각 전기적으로 분리된 별도의 전극 층에 의해 코팅된다. 제안된 이온트랩 칩은 표유전계가 강하게 발생하는 절연층 충전 실험에서 이온의 이탈을 방지하기 위해 포획 깊이 (trap depth) 를 최대화 할 수 있게 설계 되었다. 전극 표면의 산화막

존재 여부에 따른 표유전계를 평가하기 위해, 알루미늄 전극을 사용한 이온트랩 칩과 알루미늄 전극 위에 금 층을 추가로 코팅한 이온트랩 칩이 별도로 제작되었다. 174 이터븀 이온을 포획하기 위한 진공 챔버, 전기 설비, 광학 설비 등이 준비되었으며, 이 실험 환경과 제작된 칩들을 이용하여 174 이터븀 이온을 성공적으로 포획하였다. 절연층 노출 여부와 전극 표면 물질에 따른 표유전계의 세기를 평가하기 위해, 355-nm 펄스 레이저를 이온트랩 칩 표면에 주사하여 의도적으로 절연층 충전을 발생시켰다. 이 때 발생하는 이온의 위치 이동을 측정하여, 표유전계를 추정하였다. 알루미늄 전극과 드러난 절연층 측벽을 가진 이온트랩 칩의 경우 3.53 V/m 의 표유 전계 세기의 표준편차를 보였다. 알루미늄 전극으로 절연층 측벽을 보호한 이온트랩 칩의 경우 5.63 V/m 의 표유 전계 세기의 표준편차를 보였다. 금 전극으로 절연층 측벽과 칩 표면을 보호한 이온트랩 칩의 경우 1.56 V/m 의 표유 전계 세기의 표준편차를 보였다. 특히, 전극 표면과 측벽에 레이저가 인가 되었을 때는 표유 전계가 거의 유발되지 않았다. 이러한 실험 결과는 제안된 구조가 전하 충전 방지에 효과적임을 보여준다.

주요어 : 이온트랩, 미세공정, 양자정보처리, 절연층 충전, 표유전계

학번 : 2011-30979